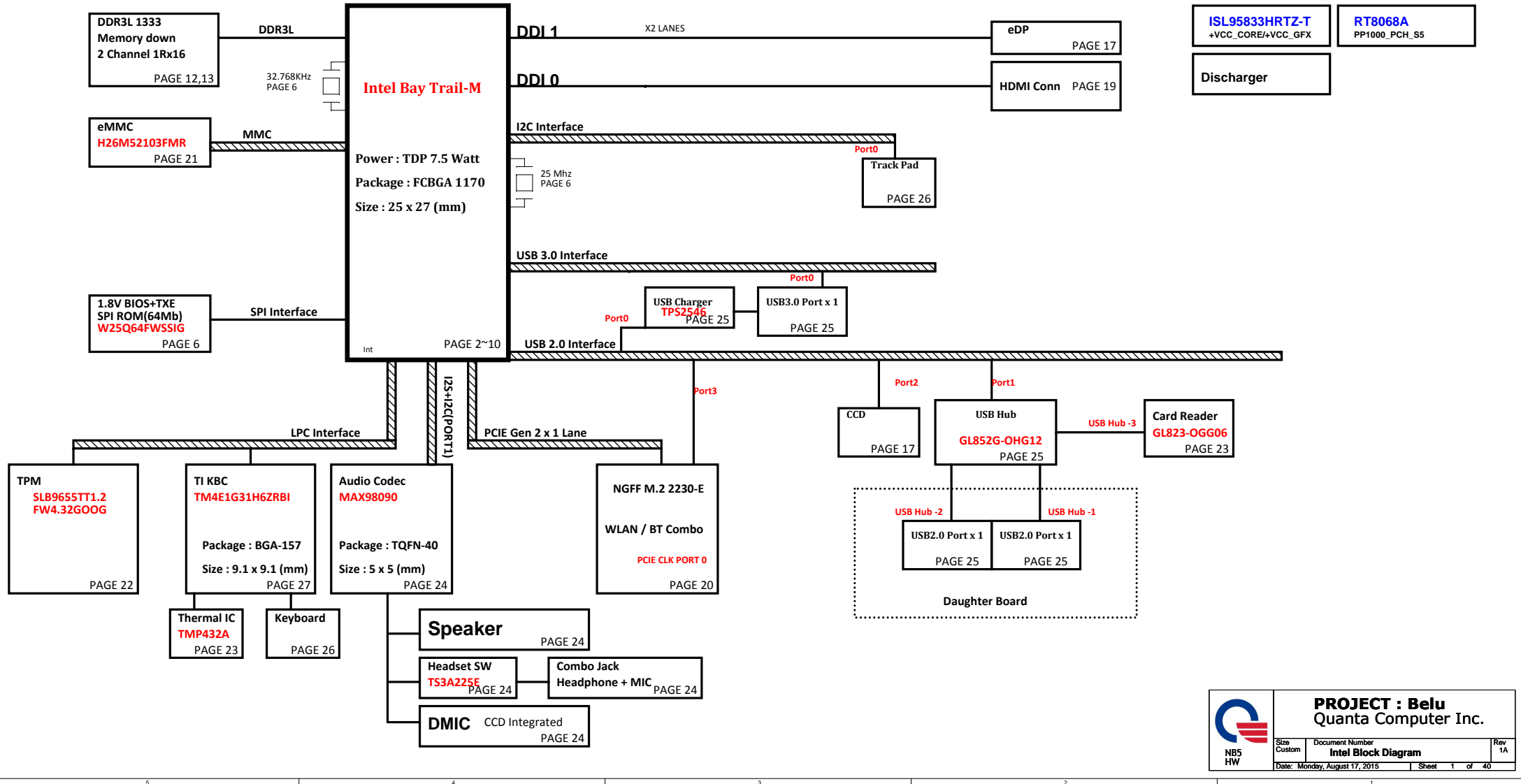
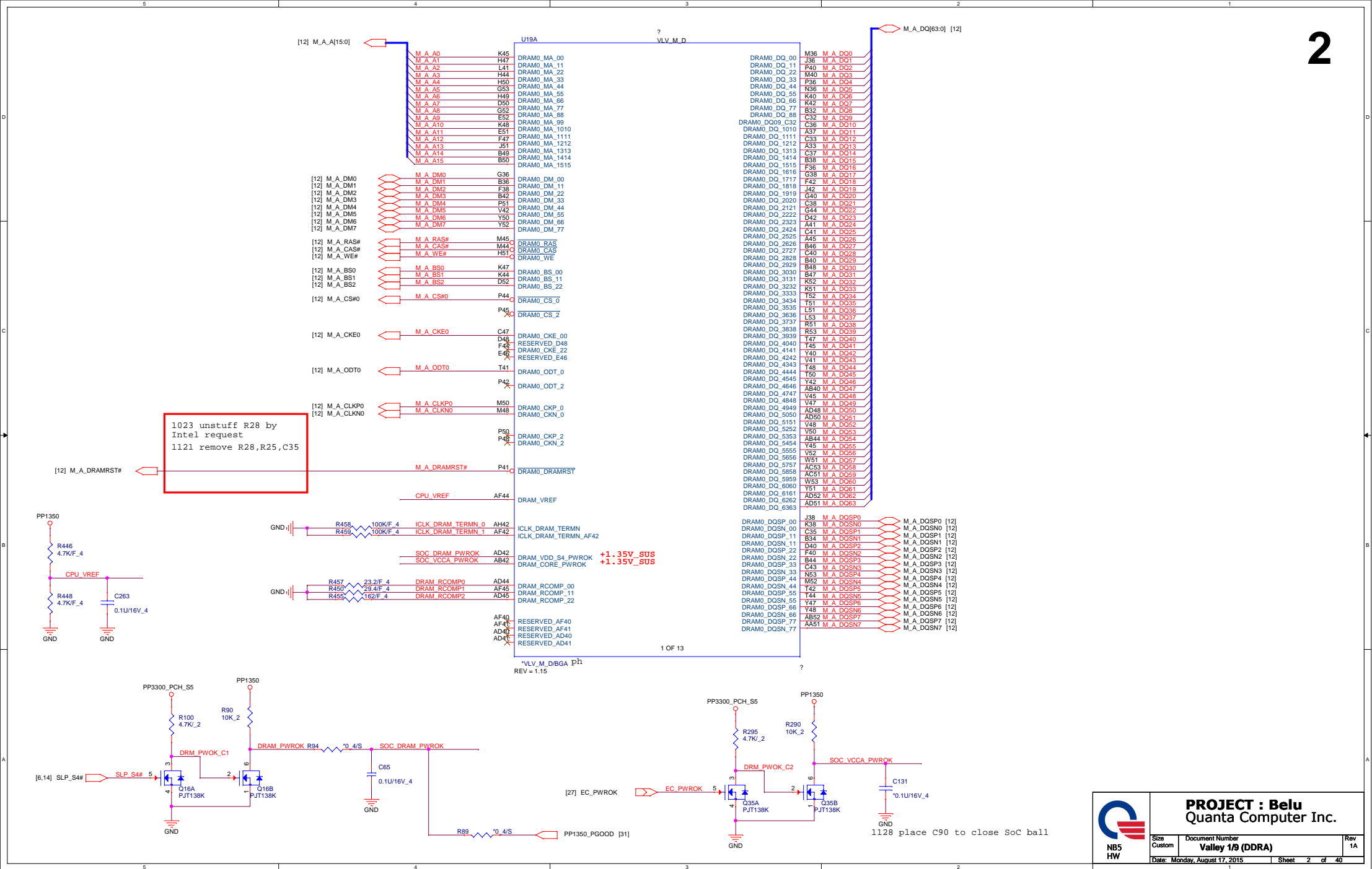
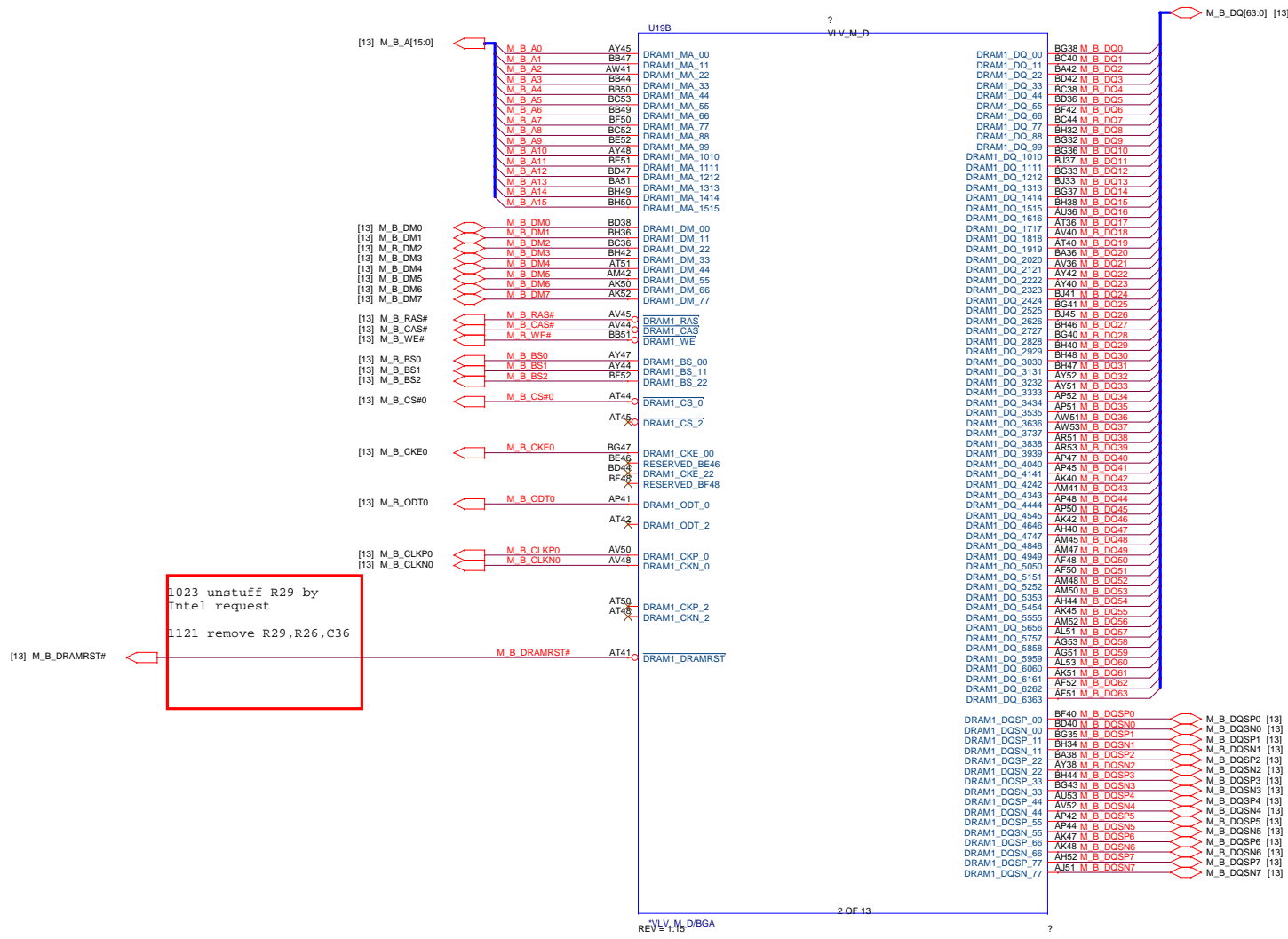


Intel Bay Trail-M Platform Block Diagram





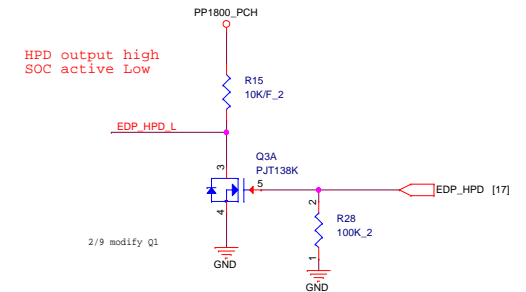


1023 unstuff R29 by Intel request

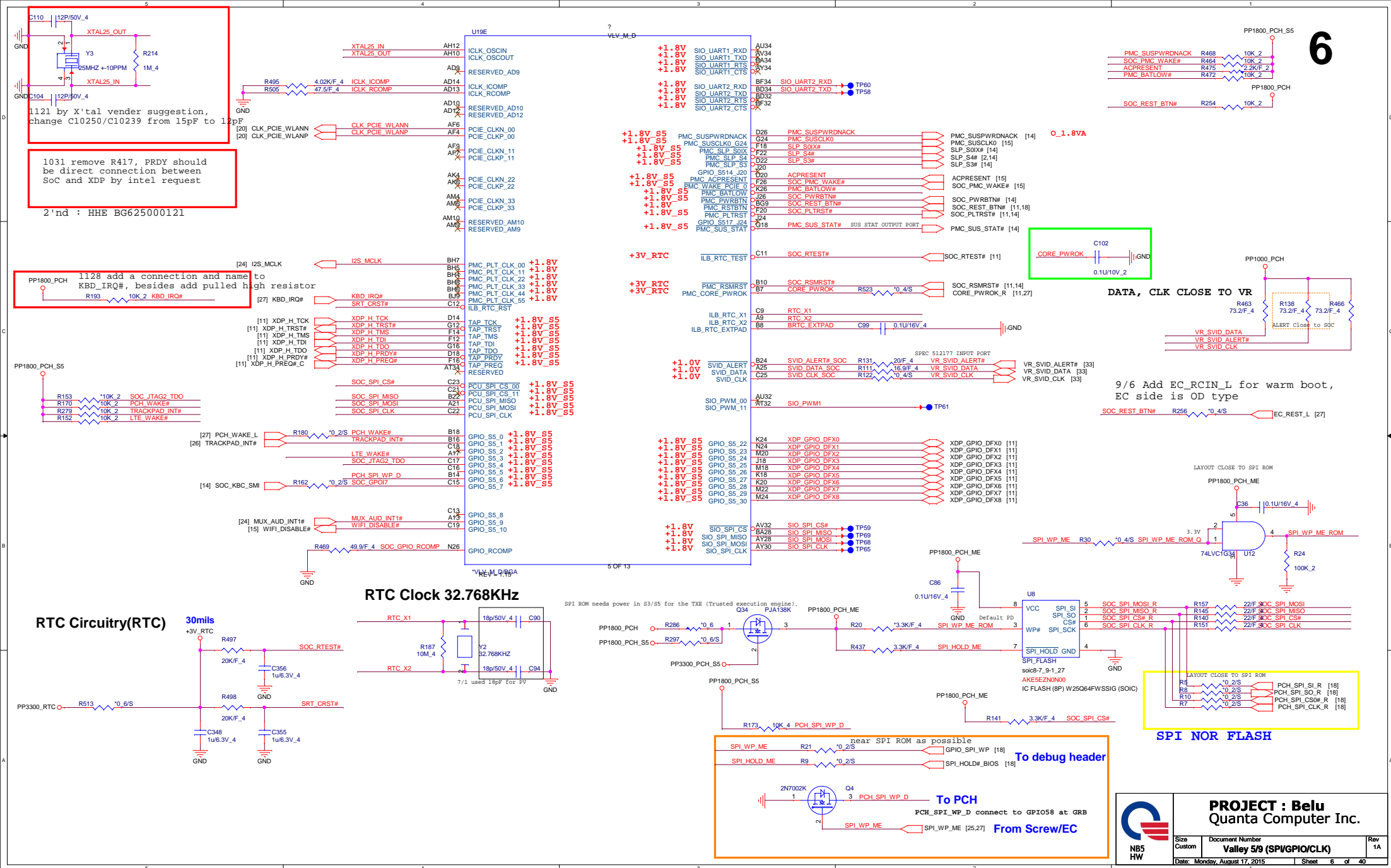
1121 remove R29,R26,C36

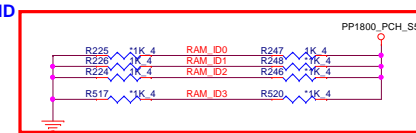
BTM Strapping Table

Pin Name	Strap description	Sampled	Configuration	Note
GPIO_SO_SC_56	Top Swap (A16 Override)	PWROK	0 = Top address bit is unchanged 1 = Top address bit is inverted	
LPE_I2S2_FRM	BIOS Boot Selection	PWROK	0 = LPC 1 = SPI	
GPIO_SO_SC_65	Security Flash Descriptors	PWROK	0 = Override 1 = Normal operation	
DDI0_DDCDATA	DDI0 Detect	PWROK	0 = DDI0 not detected 1 = DDI0 detected	Pull up +1.8V at HDMI side
DDI1_DDCDATA	DDI1 Detect	PWROK	0 = DDI0 not detected 1 = DDI0 detected	
GPIO_SO_NC_13				







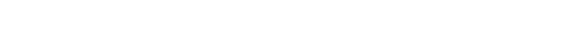
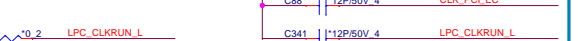
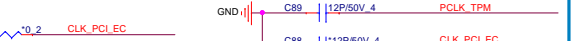
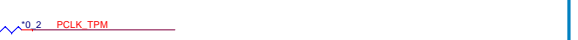
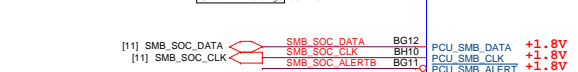
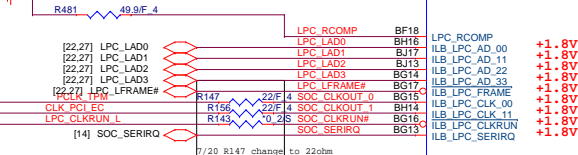
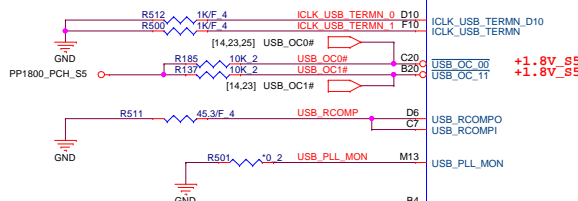


Freq. 1600MHz

Vender	RAM_ID(3,2,1,0)	TOP B/S PN	Mfr. PN	Channel	Size
Hynix	X001	AKD5JGETW07	H5TC4G63AFR-PBA	2CH	4GB
Elpida	X010	N/A	EDJ4216EFBG-GNL-F	2CH	4GB
SAMSUNG	X011	AKD5PGST508	K4B4G1646Q-HYK0	2CH	4GB
Micron E die	X000	AKD5JGSTL06	MT41K256M16HA-125:E	2CH	4GB
Elpida	X110	AKD5JGST410	EDJ4216EFBG-GNL-F	1CH	2GB
Hynix	X101	AKD5JGETW07	H5TC4G63AFR-PBA	1CH	2GB
SAMSUNG	X111	AKD5PGST508	K4B4G1646Q-HYK0	1CH	2GB
Micron Edie	X100	AKD5JGSTL06	MT41K256M16HA-125:E	1CH	2GB
Micron N die	1100	AKD5PGSTL18	MT41K256M16LY-107:N	1CH	2GB
Micron N die	1000	AKD5PGSTL18	MT41K256M16LY-107:N	2CH	4GB

PORT 1 USB CONN
PORT 2 USB CONN
PORT 3 Card Reader

MB USB3.0
HUB1
CCD
BT



+1.8V GPIO_S0_SC_55
+1.8V GPIO_S0_SC_56
+1.8V GPIO_S0_SC_57
+1.8V GPIO_S0_SC_58
+1.8V GPIO_S0_SC_59
+1.8V GPIO_S0_SC_60
+1.8V GPIO_S0_SC_61

+1.8V ILB_R254_SPKR

+1.8V SIO_I2C0_DATA
+1.8V SIO_I2C0_CLK

+1.8V SIO_I2C1_DATA
+1.8V SIO_I2C1_CLK

+1.8V SIO_I2C2_DATA
+1.8V SIO_I2C2_CLK

+1.8V SIO_I2C3_DATA
+1.8V SIO_I2C3_CLK

+1.8V SIO_I2C4_DATA
+1.8V SIO_I2C4_CLK

+1.8V SIO_I2C5_DATA
+1.8V SIO_I2C5_CLK

+1.8V SIO_I2C6_DATA
+1.8V SIO_I2C6_CLK

GPIO_S0_SC_092
GPIO_S0_SC_093

GPIO_S0_SC_092
GPIO_S0_SC_093

GPIO_S0_SC_092
GPIO_S0_SC_093

GPIO_S0_SC_092
GPIO_S0_SC_093

GPIO_S0_SC_092
GPIO_S0_SC_093

GPIO_S0_SC_092
GPIO_S0_SC_093

GPIO_S0_SC_092
GPIO_S0_SC_093

GPIO_S0_SC_092
GPIO_S0_SC_093

GPIO_S0_SC_092
GPIO_S0_SC_093

GPIO_S0_SC_092
GPIO_S0_SC_093

GPIO_S0_SC_092
GPIO_S0_SC_093

GPIO_S0_SC_092
GPIO_S0_SC_093

Touch pad

Audio Codec

Light sensor(01/27 delete)

Touch panel(01/27 delete)

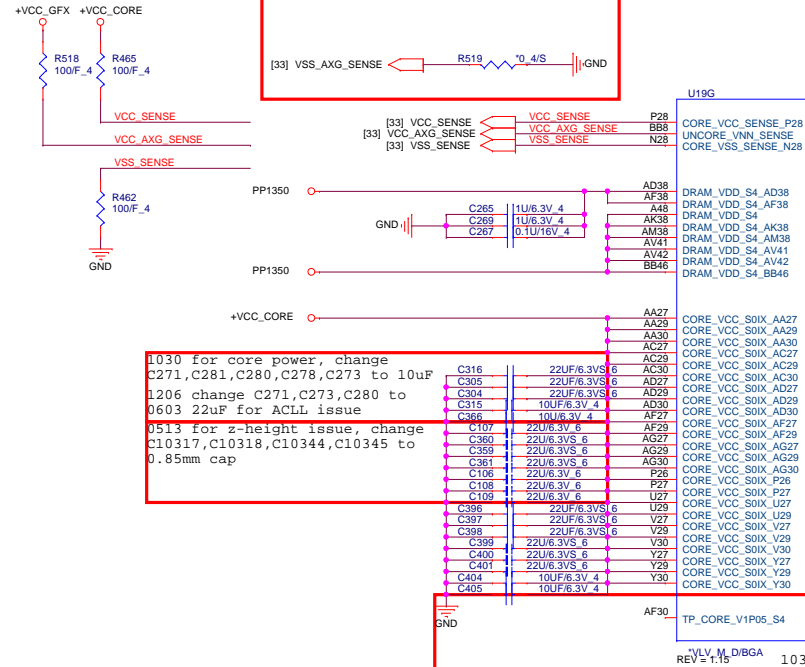


PROJECT : Belu
Quanta Computer Inc.

Size Custom Document Number Valley 6/9 (USB/LPC/I2C) Rev 1A
Date: Monday, August 17, 2015 Sheet 7 of 40

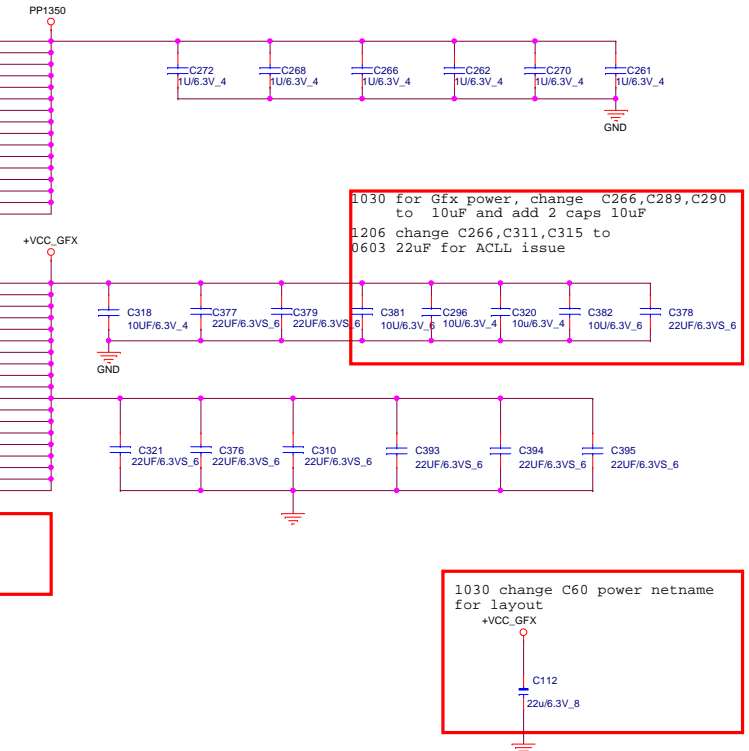
1031 for layout suggestion by intel, VSS_AXG_SENSE didn't connect to VSS_SENSE, will connect the GND via near VCC_AXG_SENSE
1031 for layout, add 0hm between GND and VSS_AXG_SENSE

[33] VSS_AXG_SENSE 



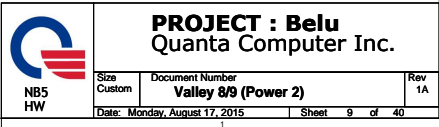
DRAM_VDD_S4_BD49
DRAM_VDD_S4_BD52
DRAM_VDD_S4_BD53
DRAM_VDD_S4_BF44
DRAM_VDD_S4_BG51
DRAM_VDD_S4_BJ48
DRAM_VDD_S4_C51
DRAM_VDD_S4_D44
DRAM_VDD_S4_F49
DRAM_VDD_S4_F52
DRAM_VDD_S4_F53
DRAM_VDD_S4_H46
DRAM_VDD_S4_M41
DRAM_VDD_S4_M42
DRAM_VDD_S4_V38
DRAM_VDD_S4_Y38

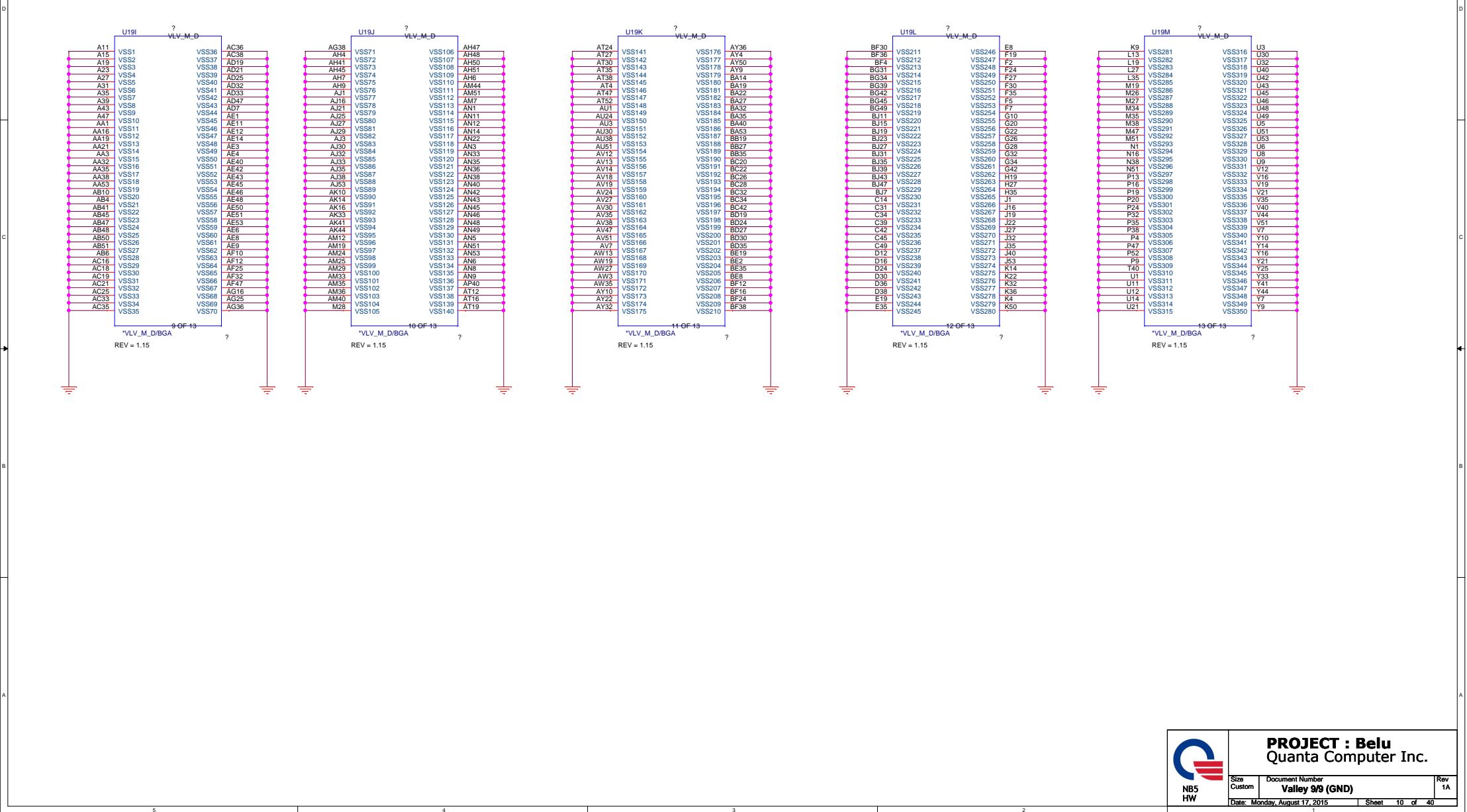
UNCORE_VNN_S3_AA24
UNCORE_VNN_S3_AC22
UNCORE_VNN_S3_AC24
UNCORE_VNN_S3_AD22
UNCORE_VNN_S3_AD24
UNCORE_VNN_S3_AF22
UNCORE_VNN_S3_AF24
UNCORE_VNN_S3_AG22
UNCORE_VNN_S3_AG24
UNCORE_VNN_S3_AJ22
UNCORE_VNN_S3_AJ24
UNCORE_VNN_S3_AK22
UNCORE_VNN_S3_AK24
UNCORE_VNN_S3_AK25
UNCORE_VNN_S3_AK27
UNCORE_VNN_S3_AK29
UNCORE_VNN_S3_AK30
UNCORE_VNN_S3_AK32
UNCORE_VNN_S3_AM22



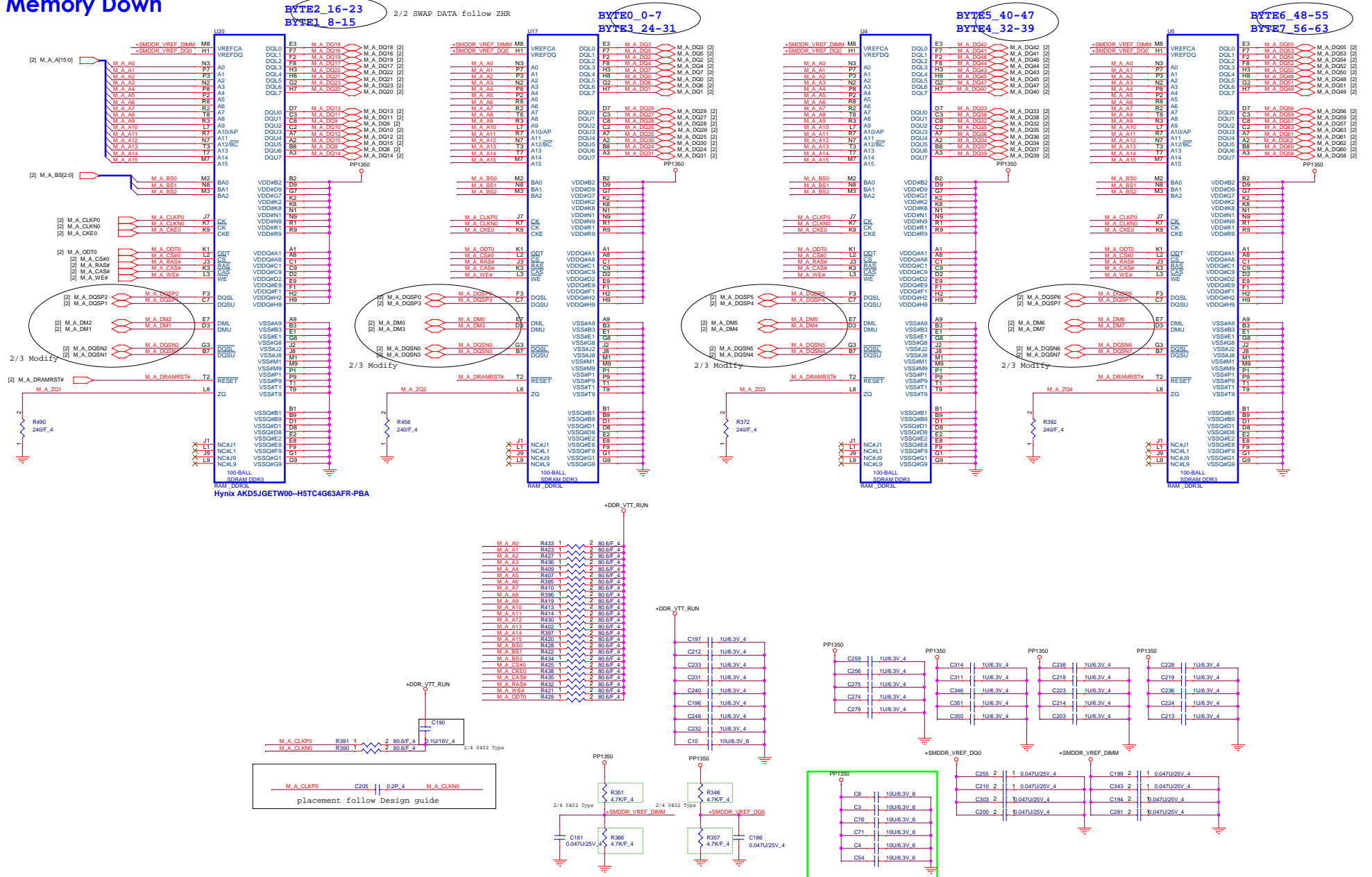
PROJECT : Belu
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Valley 7/9 (Power 1)	1A
Date: Monday, August 17, 2015	Sheet 8 of 40	





DDR3 CHA Memory Down



DDR3 CHB Memory Down

<DDR>

BYTE16_23

BYTE24_31

2/4 Modify

BYTE0_7

BYTE8_15

2/4 Modify

BYTE6_48-55

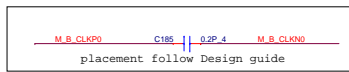
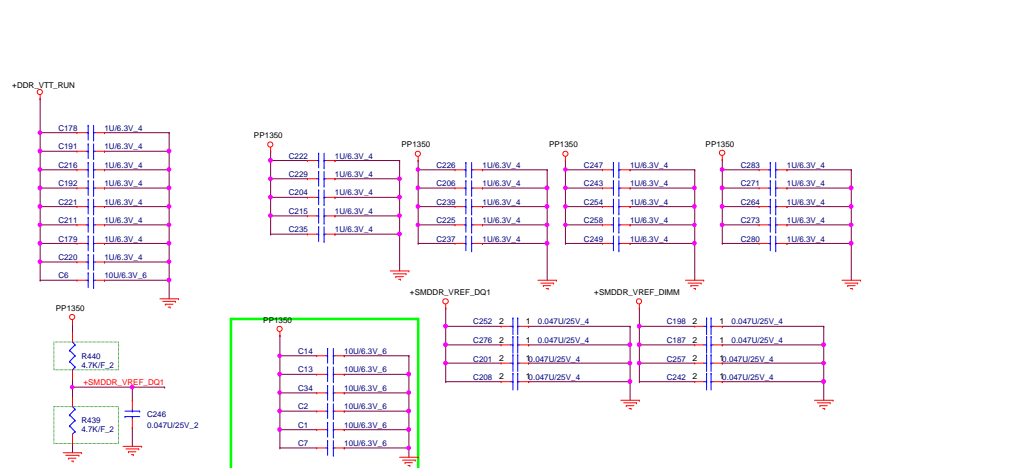
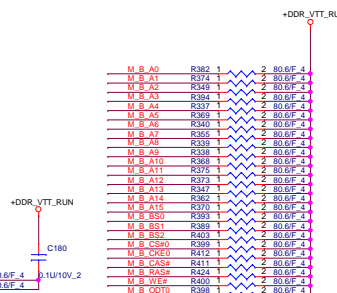
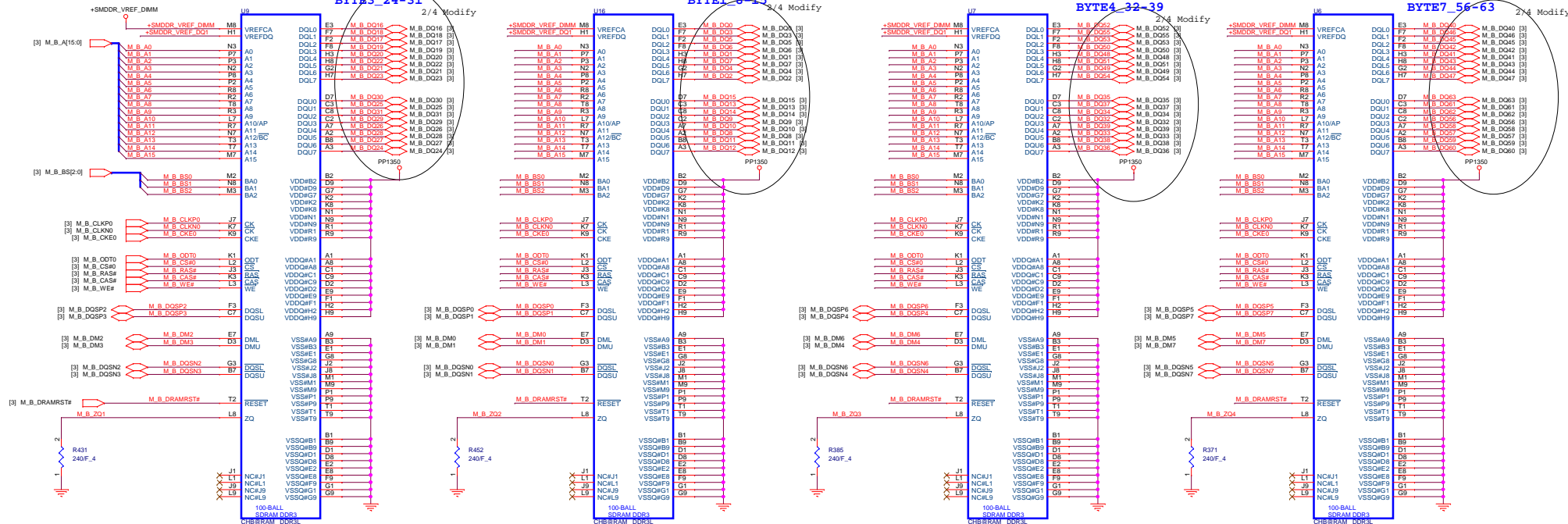
BYTE32-39

2/4 Modify

BYTE5_40-47

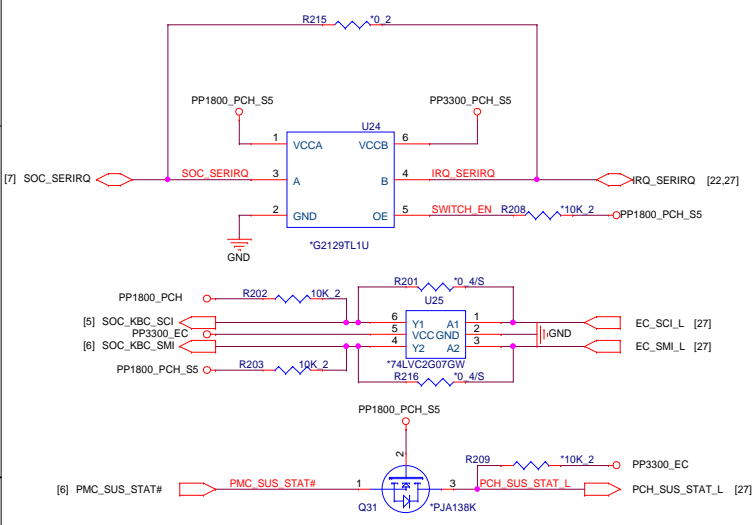
BYTE7_56-63

2/4 Modify

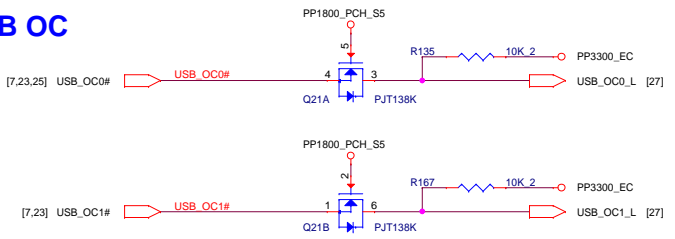


PWRON SEQUENCE

9/6 EC table says SERIRQ is OD pin, reserve for debugging
 1128 remove R166, because SERIQ of TPM needs 3V
 1128 reserve 0 ohm R387/R391 on VCCA and VCCB for debugging

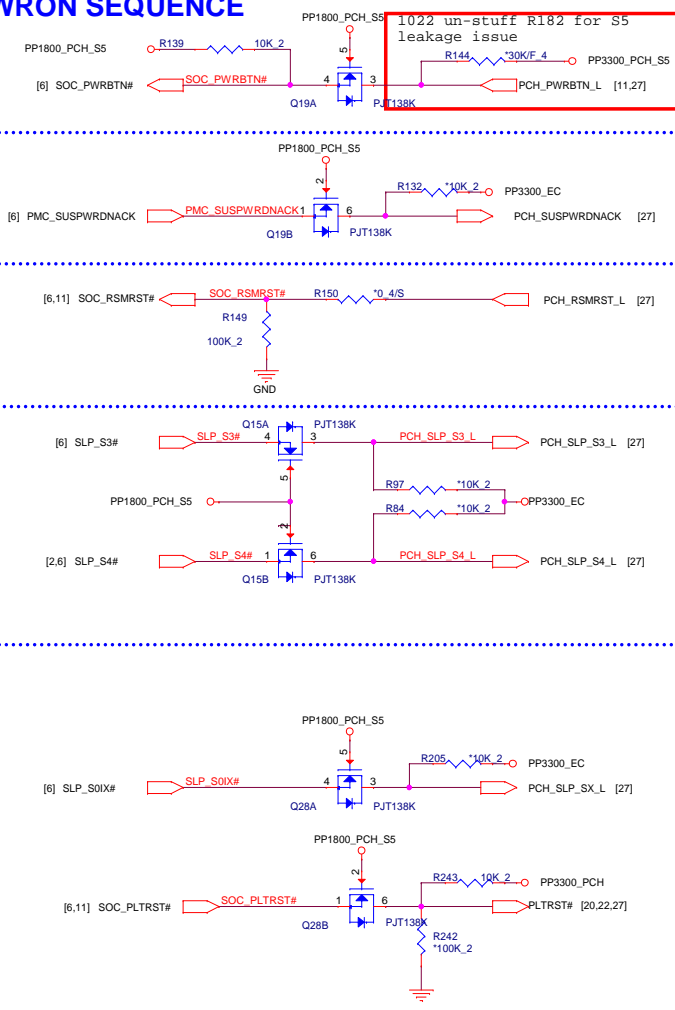


USB OC

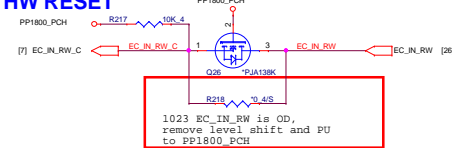
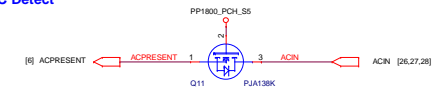


Stuffing for notifying EC

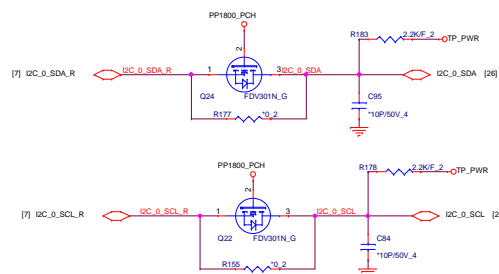
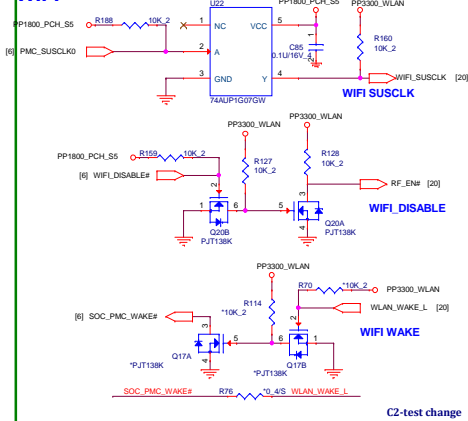
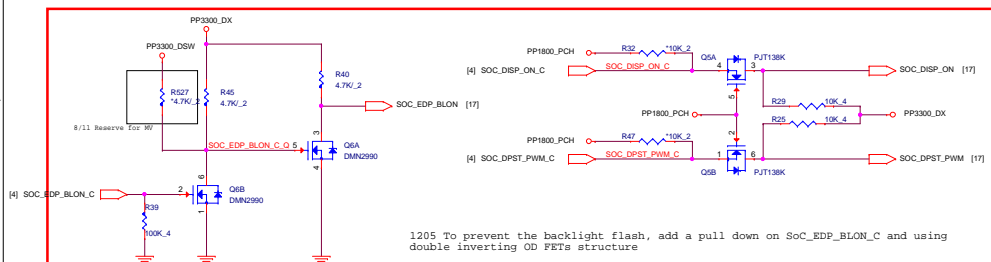
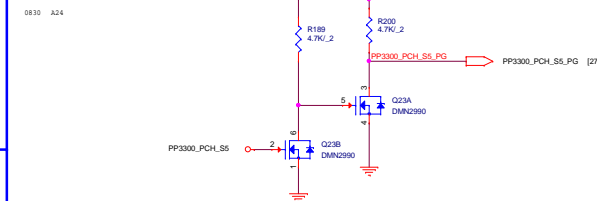
PWRON SEQUENCE



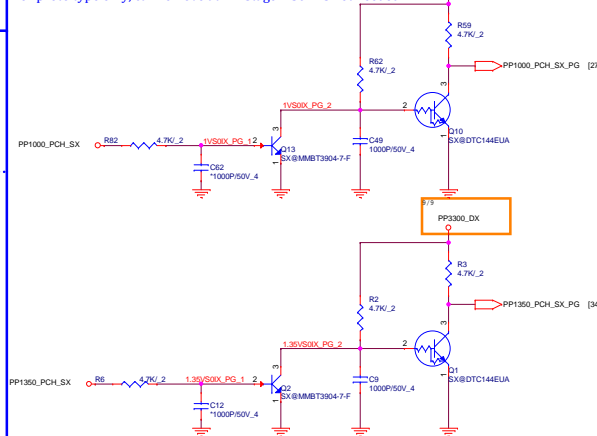
0220 remove SPI_SIO Interface,
 Q35,Q36,Q37,Q44,R486,R484,R485,
 R483,R426,R429,R427,R428

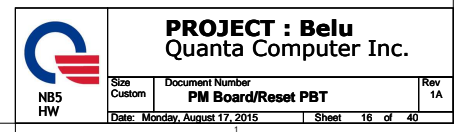
HW RESET**AC Detect****SATA**

1025 Delete complete SSD (connector and caps)

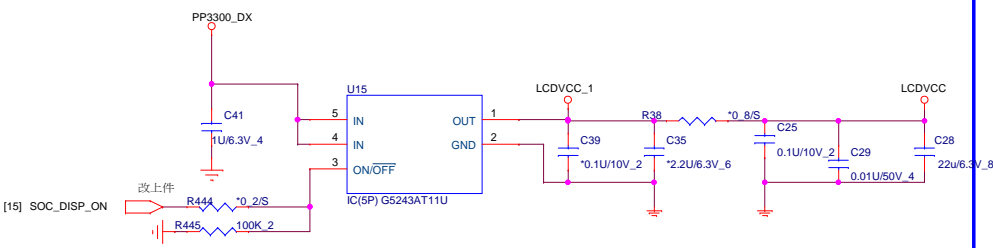
Track Pad**WIFI****eDP control pin****S5 Power Good(+3V_S5)****S0iX Power Good**

for proto type only, can remove at MP stage if S0ix is not needed

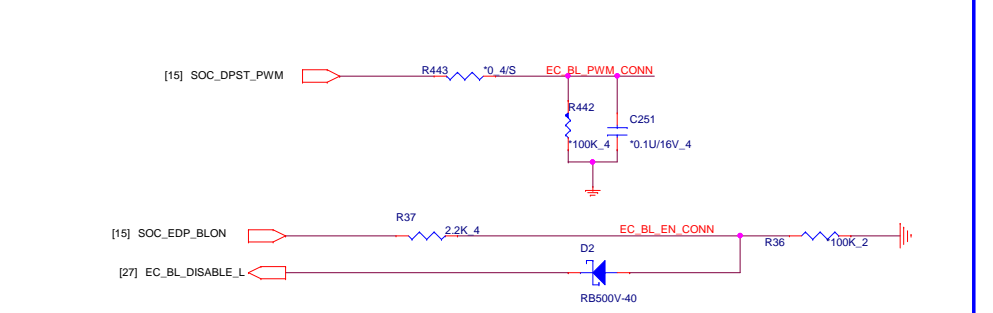




eDP Power(VGA)

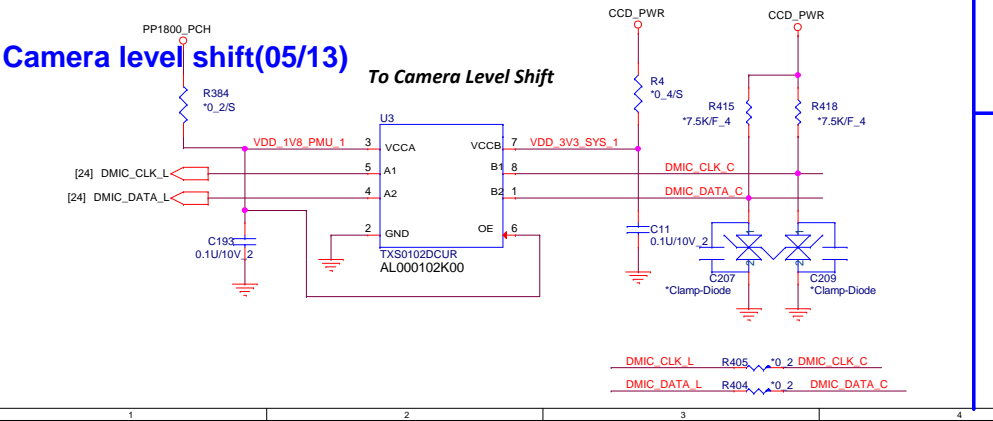


eDP panel control(VGA)

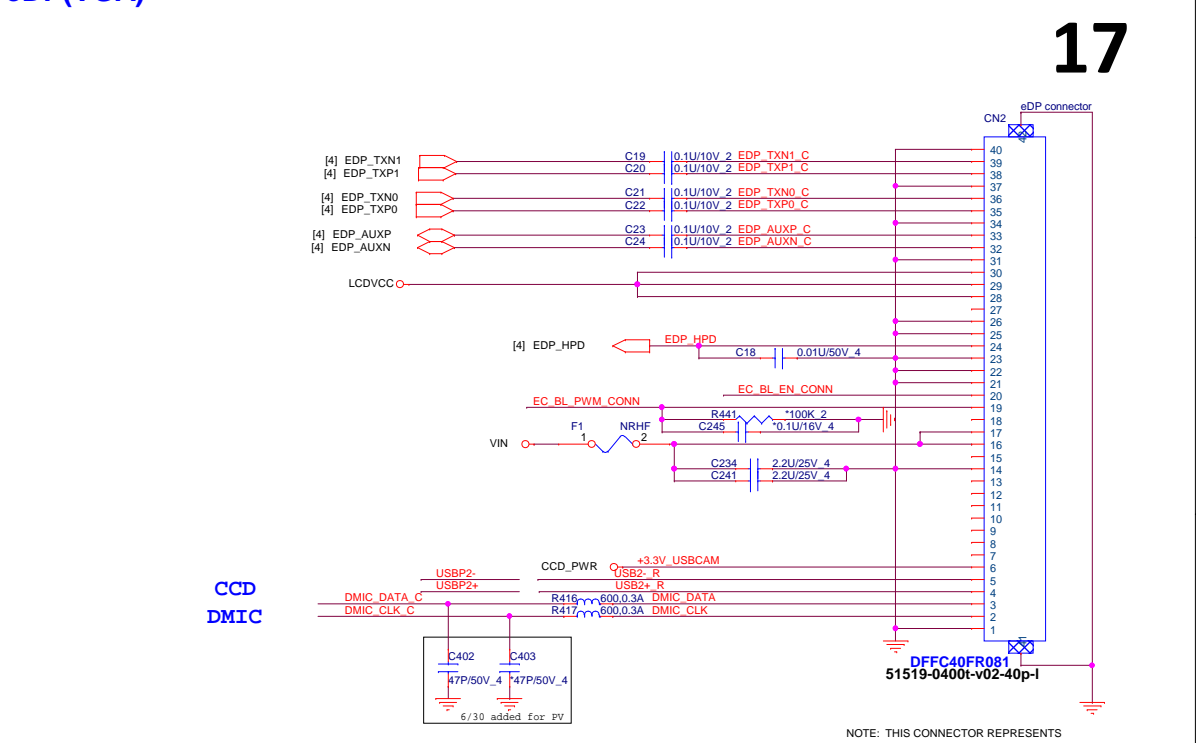


Camera level shift(05/13)

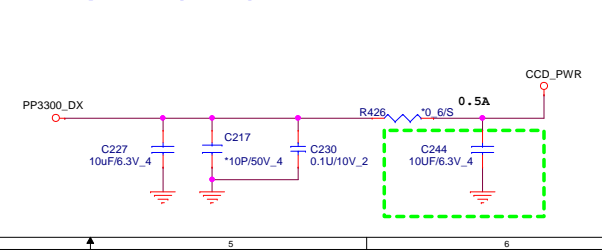
To Camera Level Shift



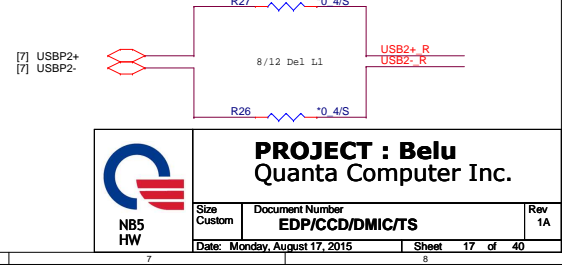
eDP(VGA)



CCD power(CCD)



CCD USB(CCD)



PROJECT : Belu Quanta Computer Inc.			
Size Custom	Document Number EDP/CCD/DMIC/TS	Rev 1A	
Date: Monday, August 17, 2015	Sheet	17	of 40

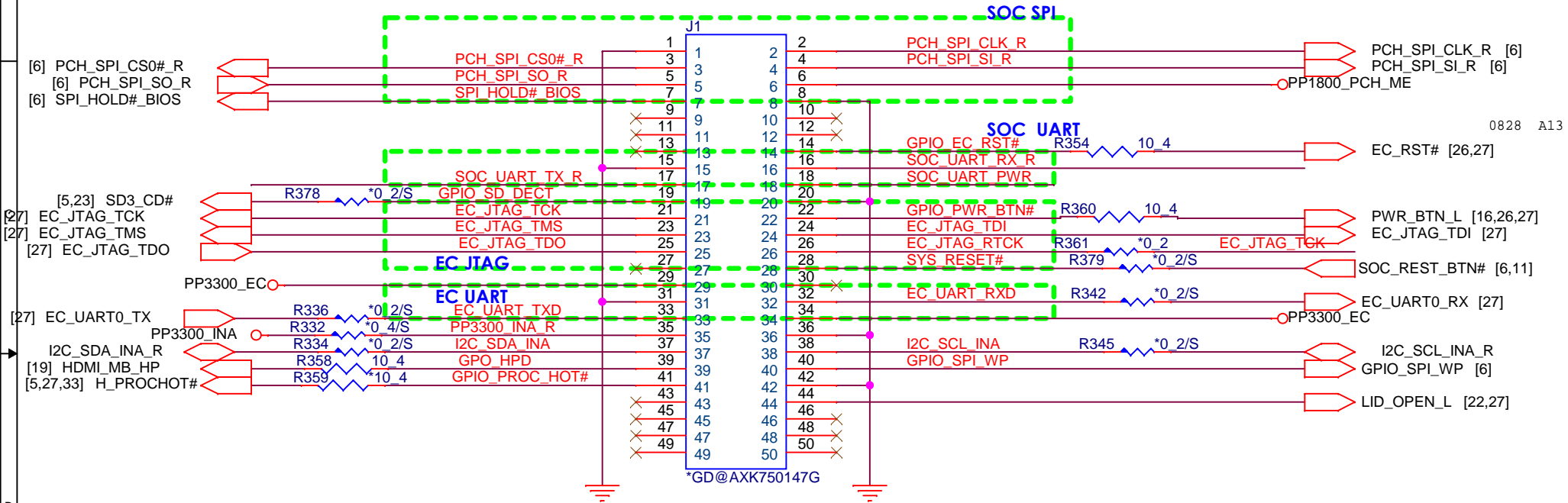
GOOGLE Debug Port(MPC)

50 pin BTB is *MUST*, don't use 42 pin

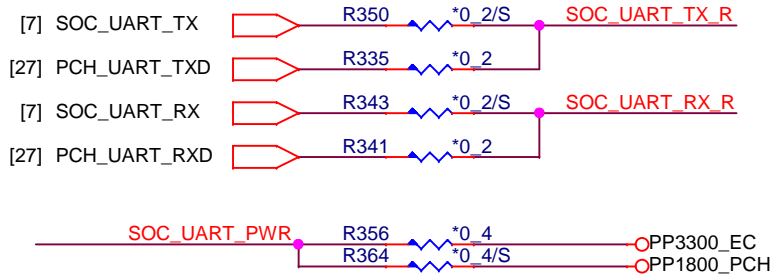
Socket part number AXK750147G

PIN7	OD	PIN39	OD	PIN49	OD
PIN14	OD	PIN41	OD	PIN50	OD
PIN19	OD	PIN43	OD		
PIN22	OD	PIN44	OD		
PIN28	OD	PIN45	OD		
PIN30	OD	PIN46	OD		
PIN37	OD	PIN47	OD		
PIN38	OD	PIN48	OD		

18

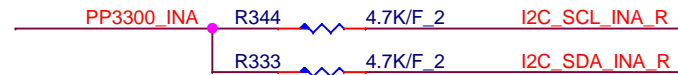


1021 change footprint and PN



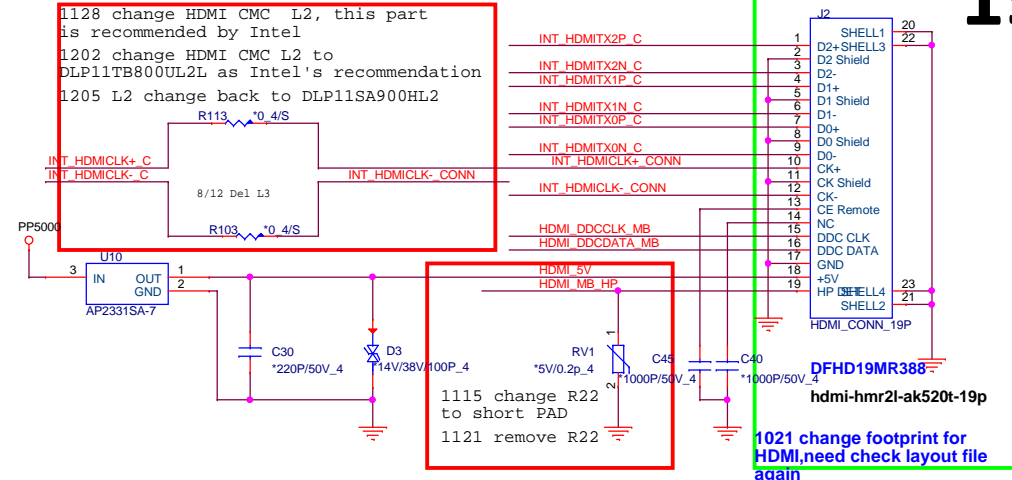
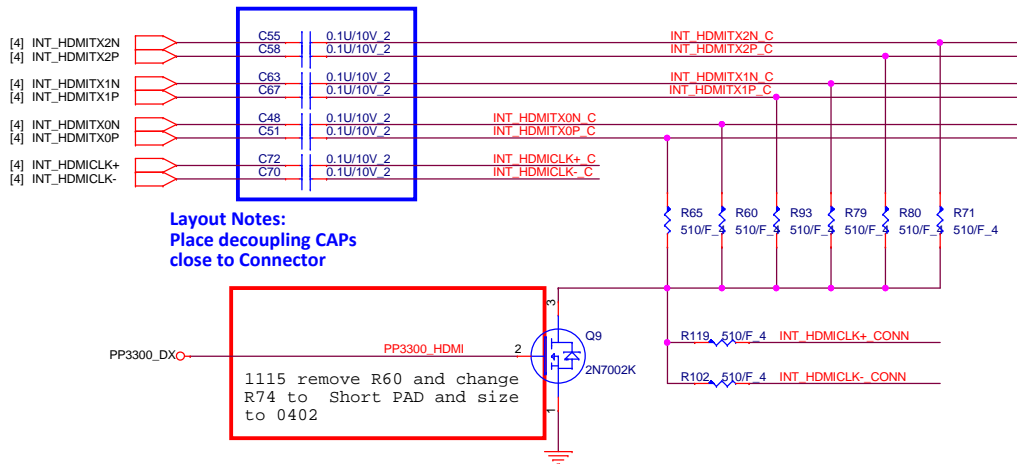
9/6 using optional instead of level shifted, default is from SoC

9/13 add pull up



PROJECT : Belu
Quanta Computer Inc.

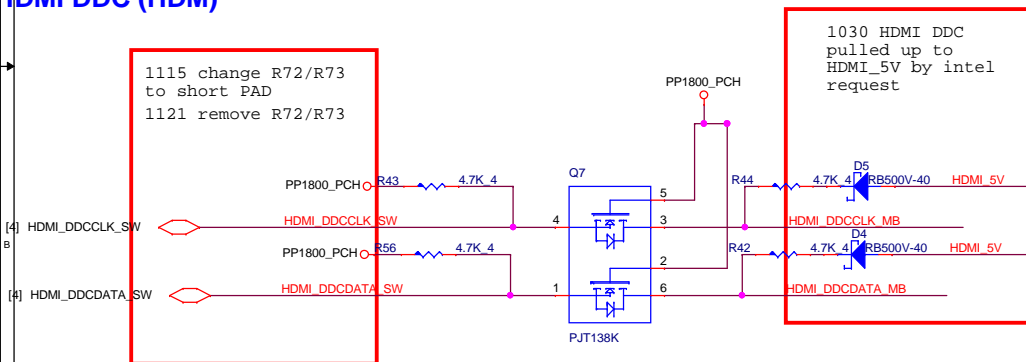
Size Custom	Document Number Google Debug	Rev 1A
Date: Monday, August 17, 2015		Sheet 18 of 40



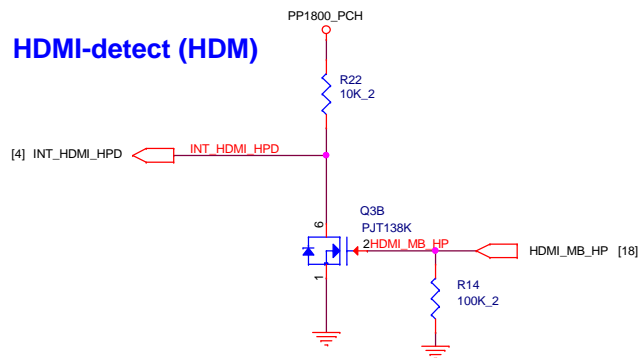
19

HDMI DDC (HDM)

HDMI DDC (HDM)

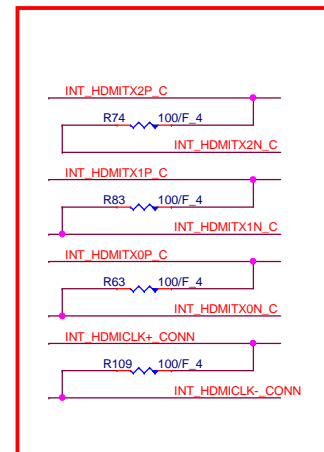


HDMI-detect (HDM)



EMI

ESD



PROJECT : Belu
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDMI	1A
Date: Monday, August 17, 2015	Sheet 19 of 40	

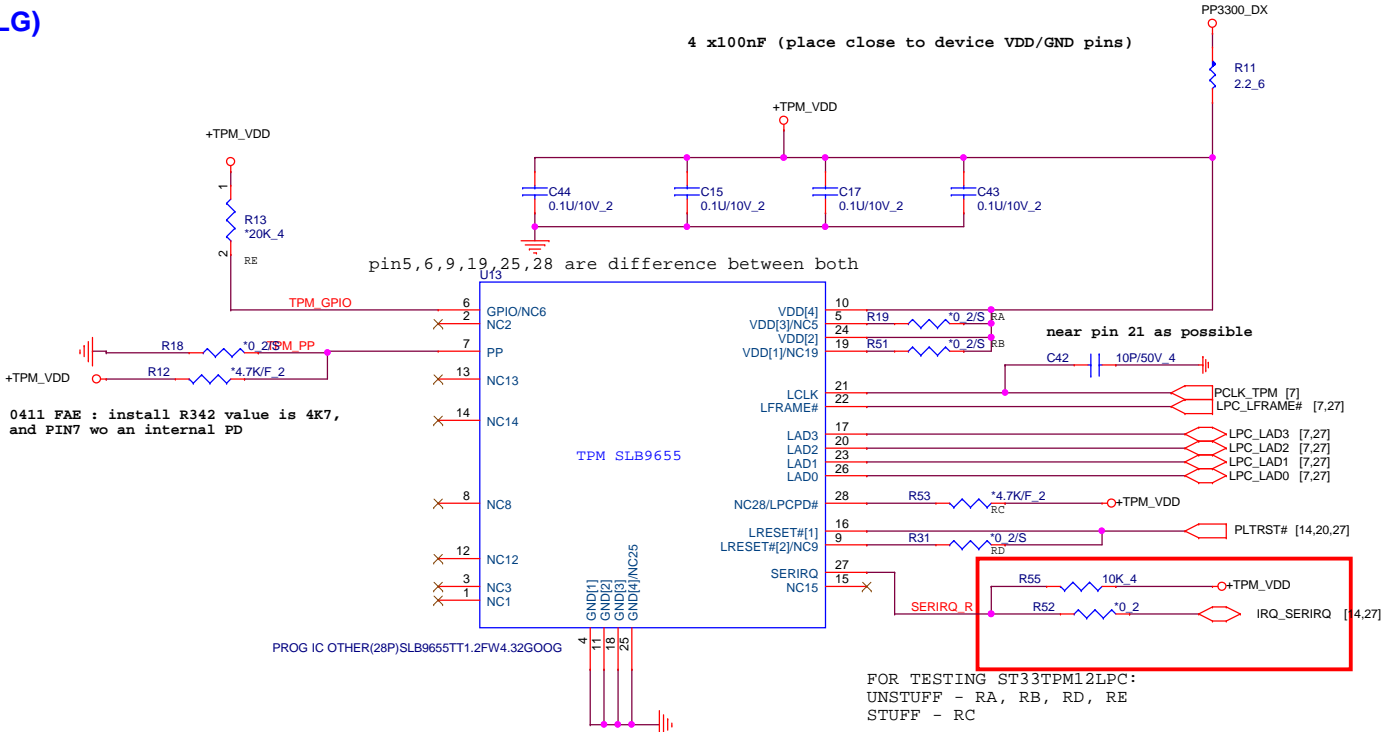


1025 Delete complete SSD(connector and caps)



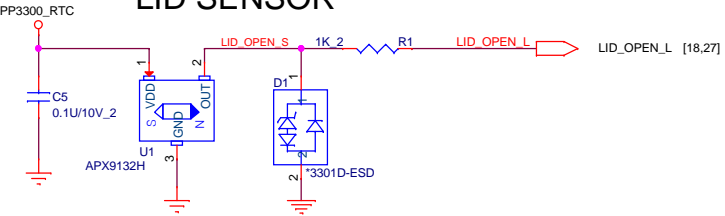
TPM (CLG)

22

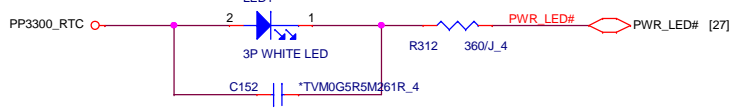


LED(UIF)

LID SENSOR

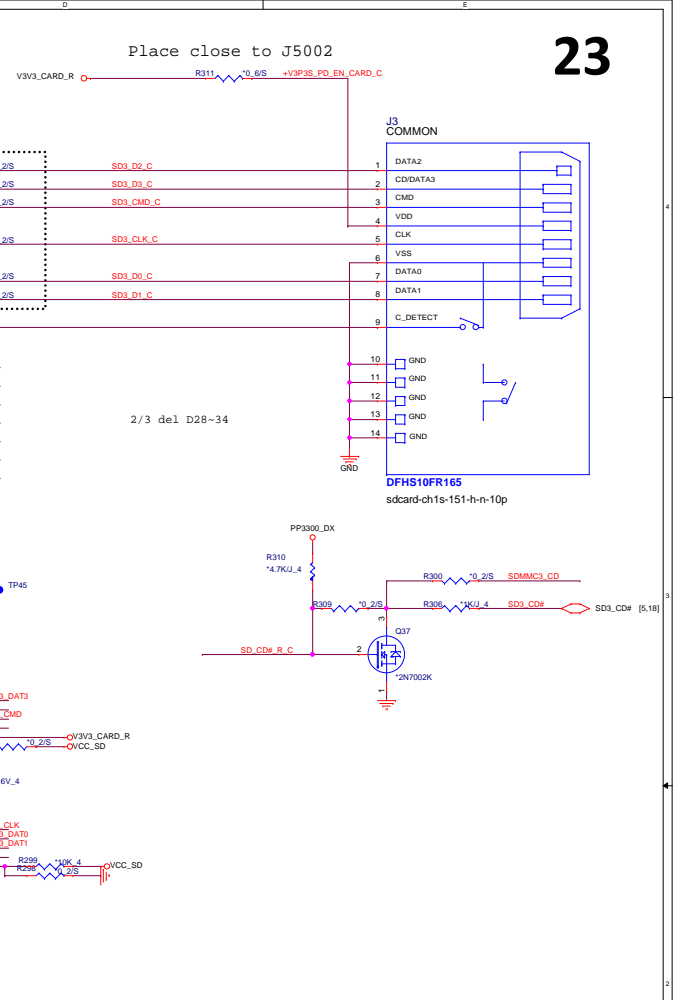
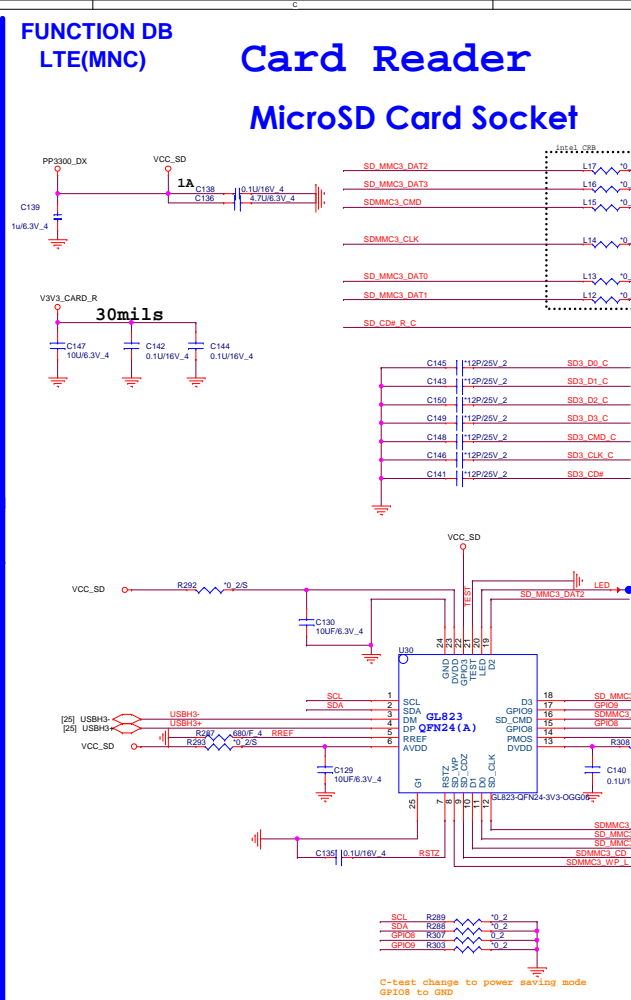
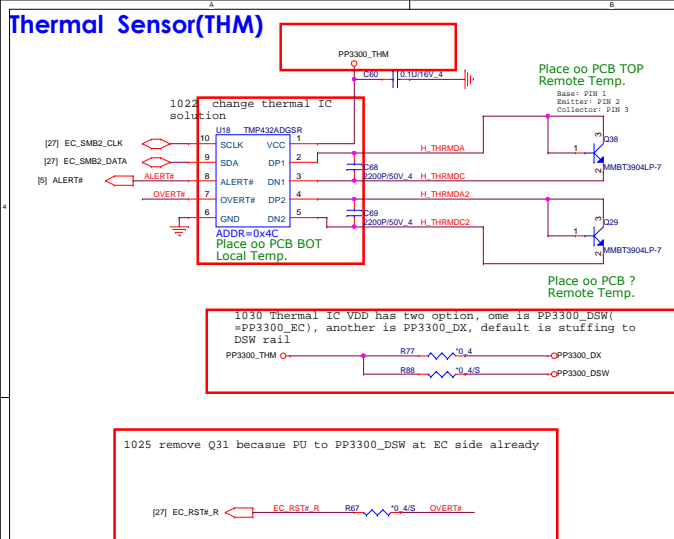


PWR LED

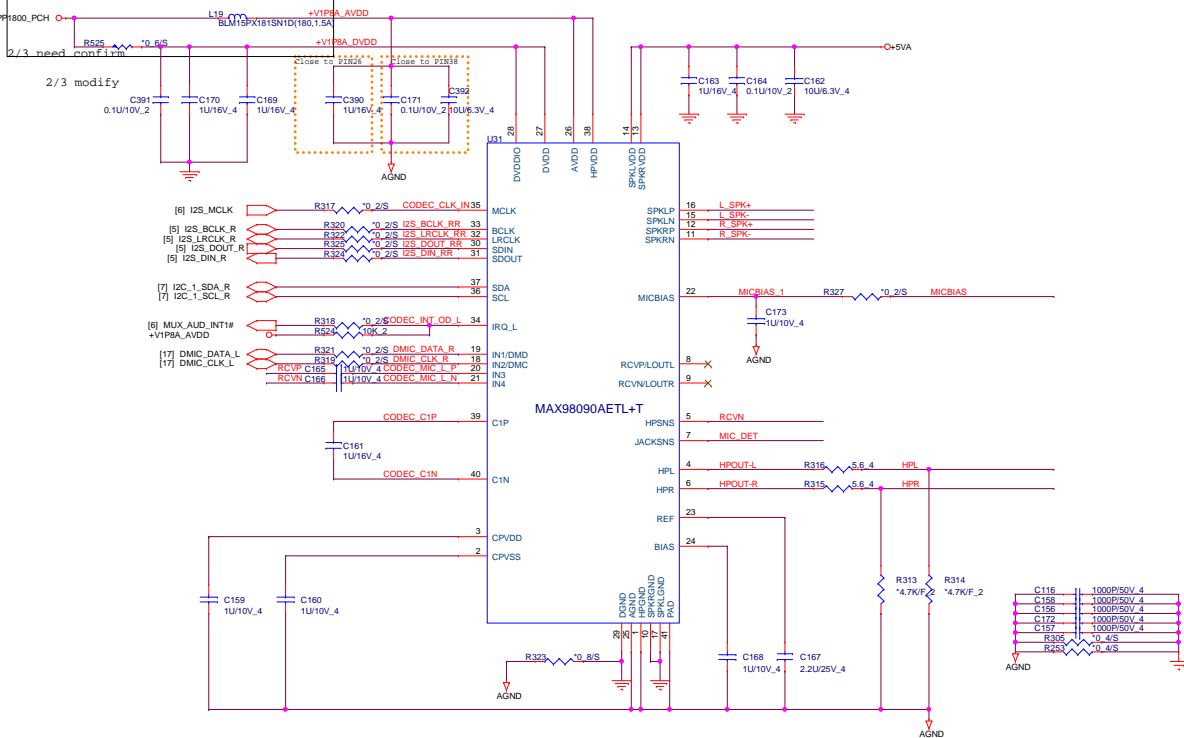


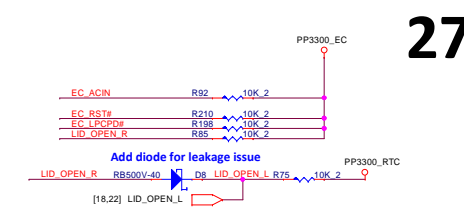
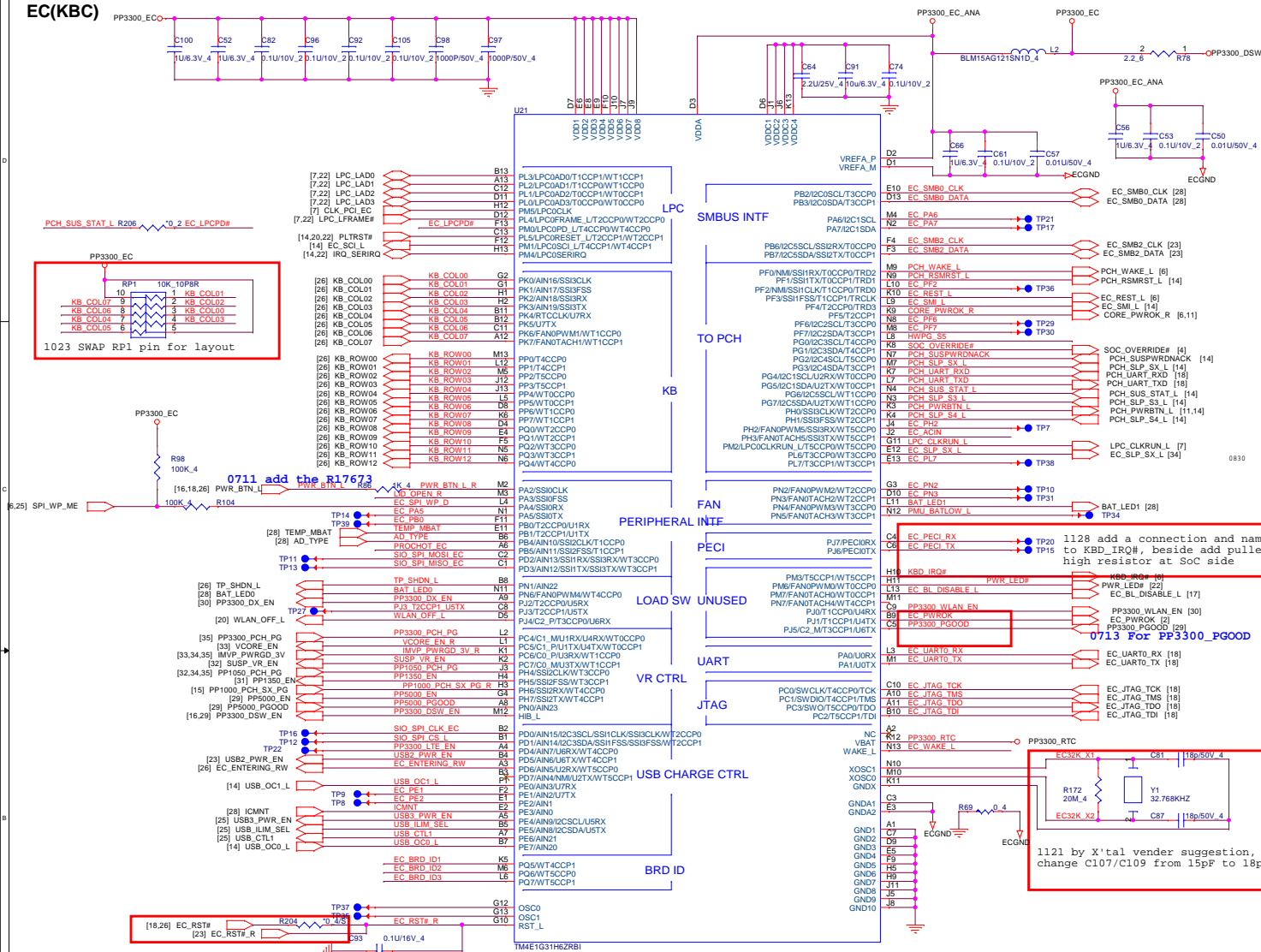
PROJECT : Belu
Quanta Computer Inc.

Size Custom	Document Number TPM SLB9655 / LED	Rev 1A
Date: Monday, August 17, 2015	Sheet 22 of 40	

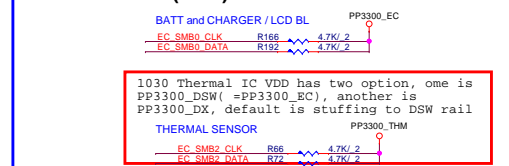


AUDIO CODEC (ADO)

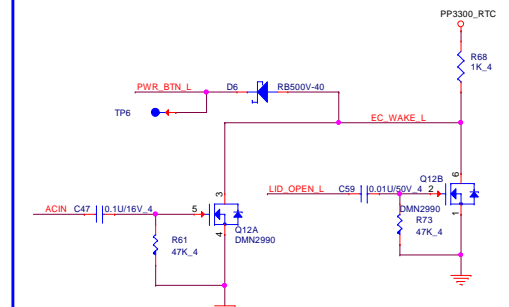




SM BUS/I2C PU(KBC)



EC HIB WAKE SOURCES



SM BUS ARRANGEMENT TABLE

SM Bus 0	BATT and CHARGER
SM Bus 1	NA
SM Bus 2	THERMAL SENSOR

HWPG(KBC)



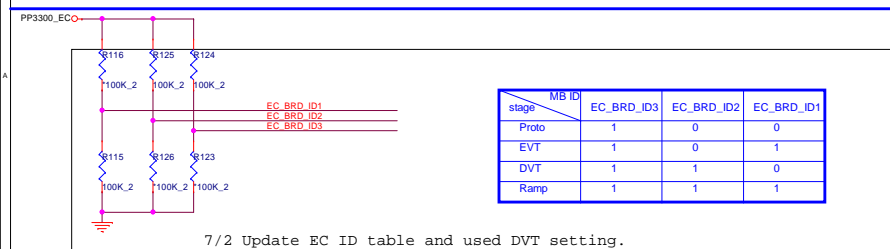
OD pin list

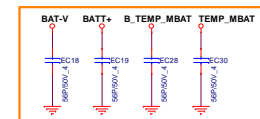
EC_REST_L
BAT_LED0
BAT_LED1
PCH_RSMRST_L
SMBUS
IRQ_SERIRQ
EC_BL_DISABLE_L

For testing only 0714 delete Power BTN



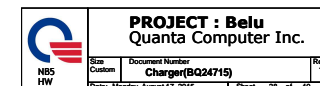
Size Custom	Document Number	Rev 1A
	KBC TI TM4E1G31H6ZRBI	
Date: Monday, August 17, 2015	Sheet	27 of 40



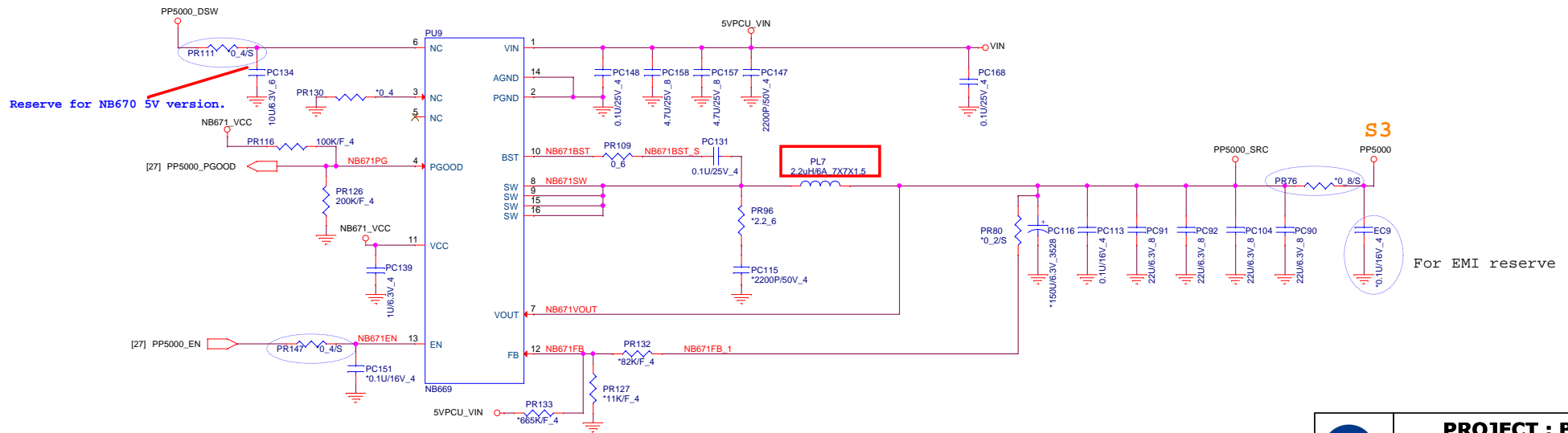
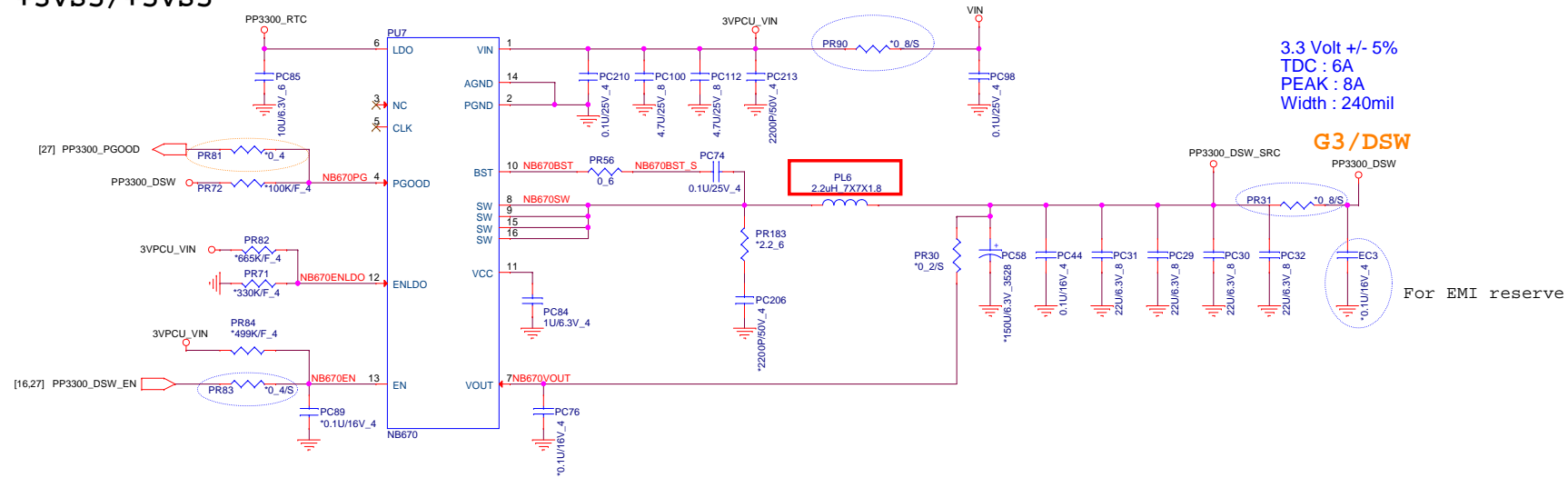


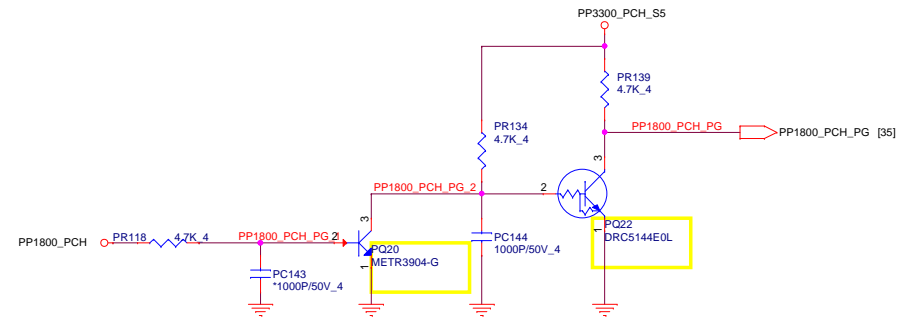
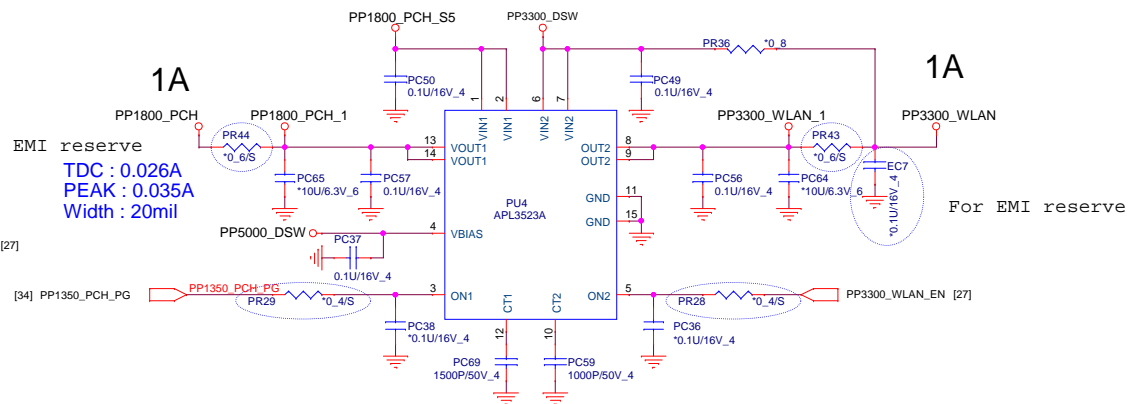
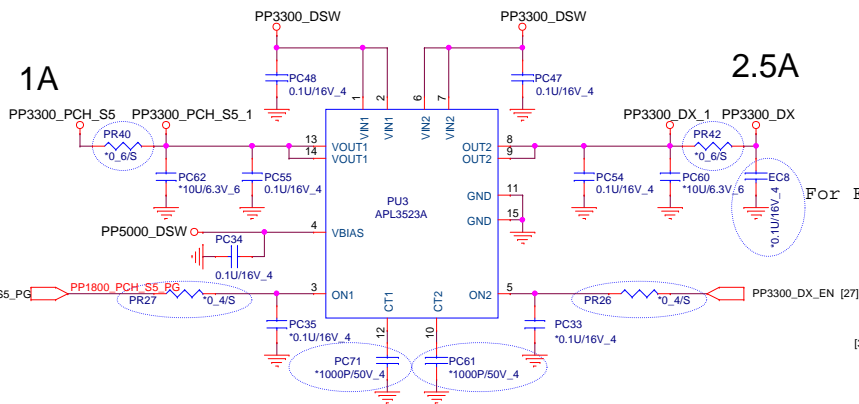
The diagram shows a parallel circuit with four capacitors labeled EC17, EC16, EC14, and EC15. Each capacitor is represented by two parallel lines and has a value of $100.25V_8$. They are connected to a voltage source labeled VCHGR_IN.

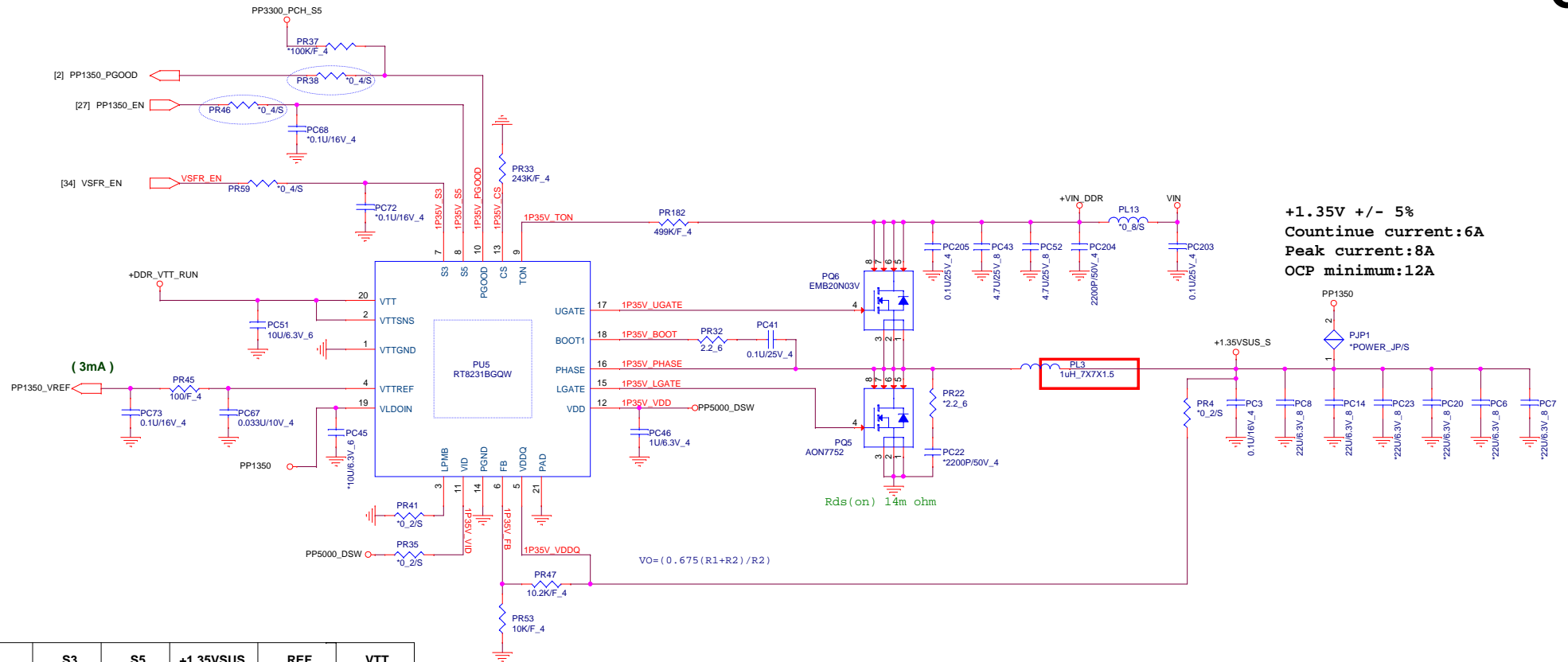
10ms one-shot circuit



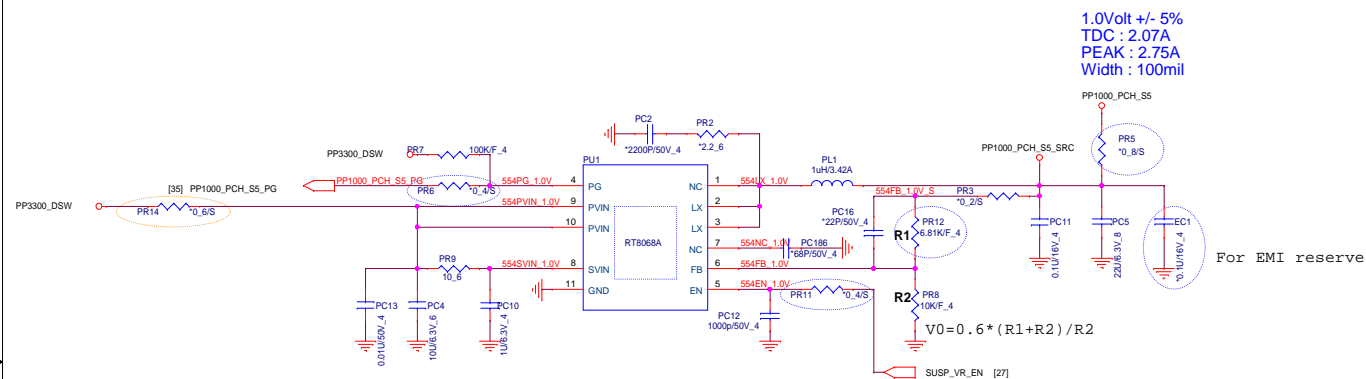
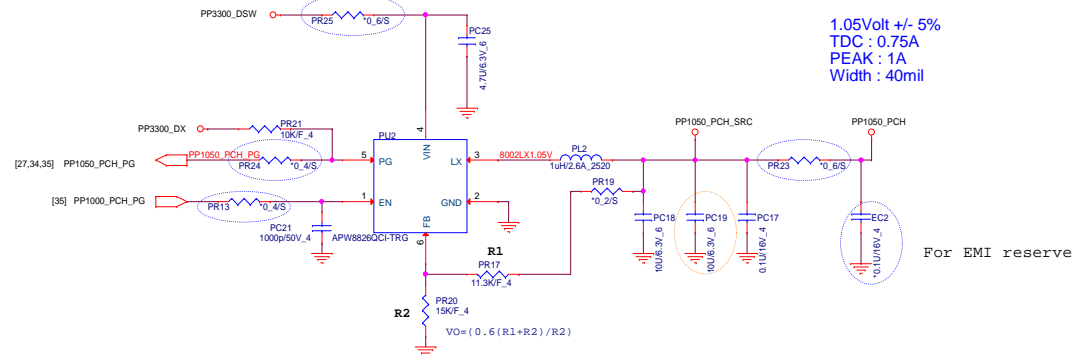
DC/DC +3VS5/+5VS5

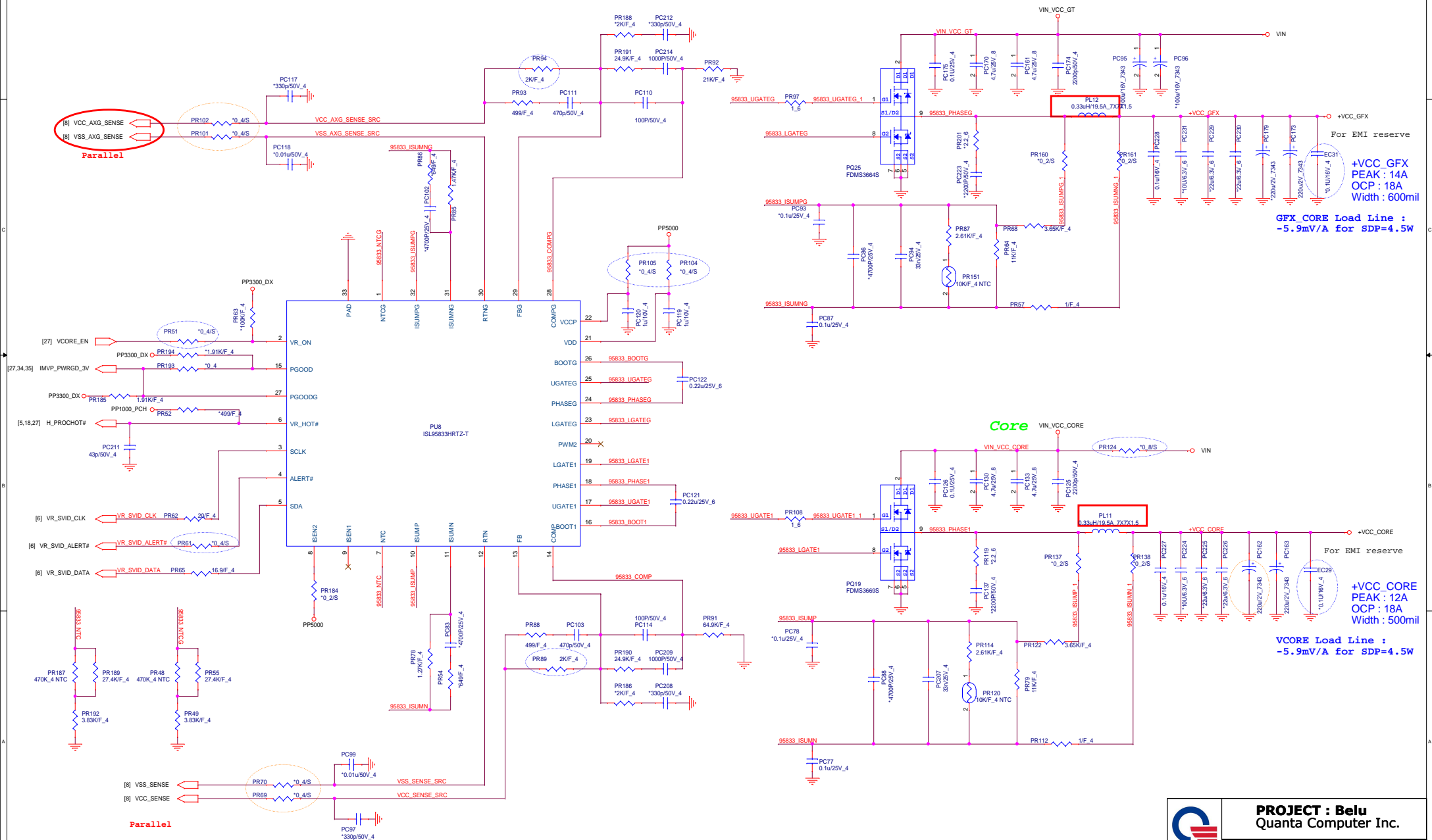









	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (main on off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

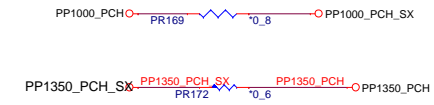
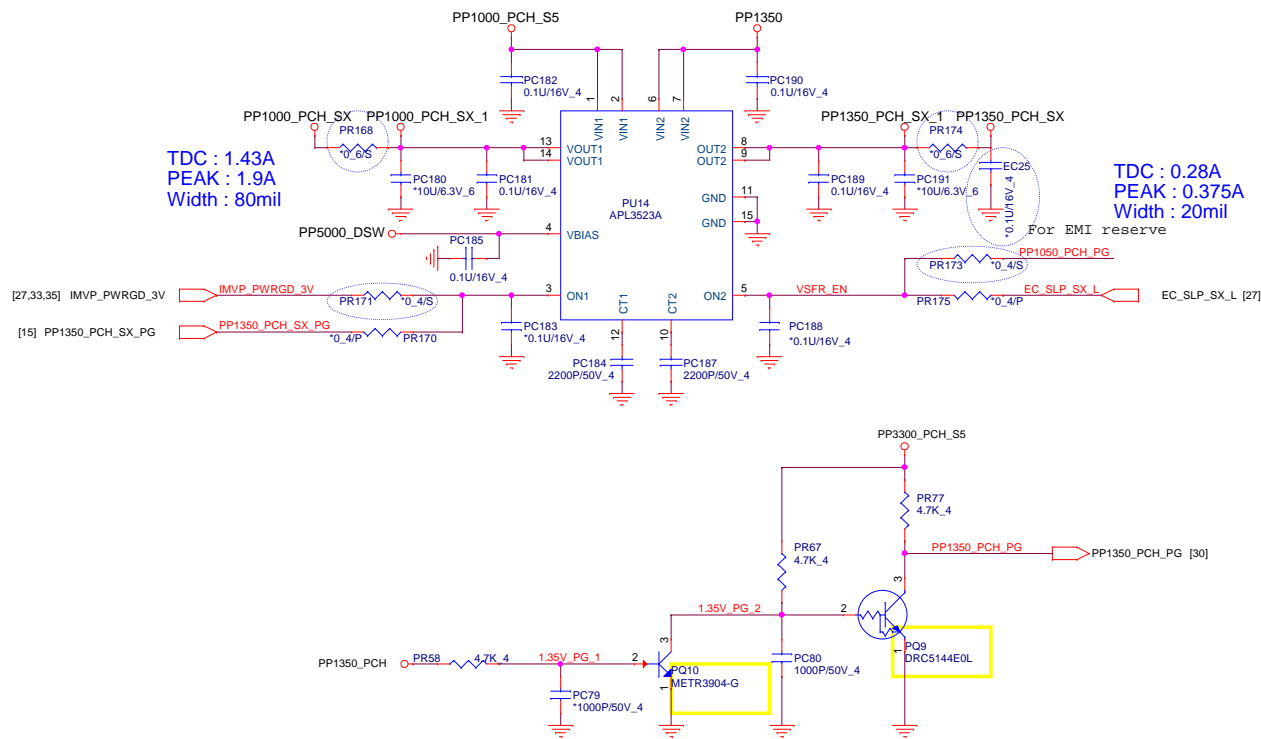




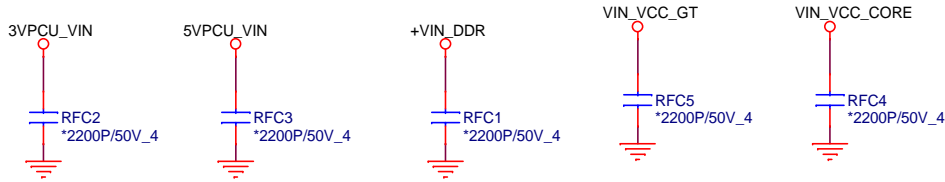
[31] VSFR_EN  VSFR_EN

[27,32] SUSP_VR_EN 

[27,32,35] PP1050_PCH_PG 



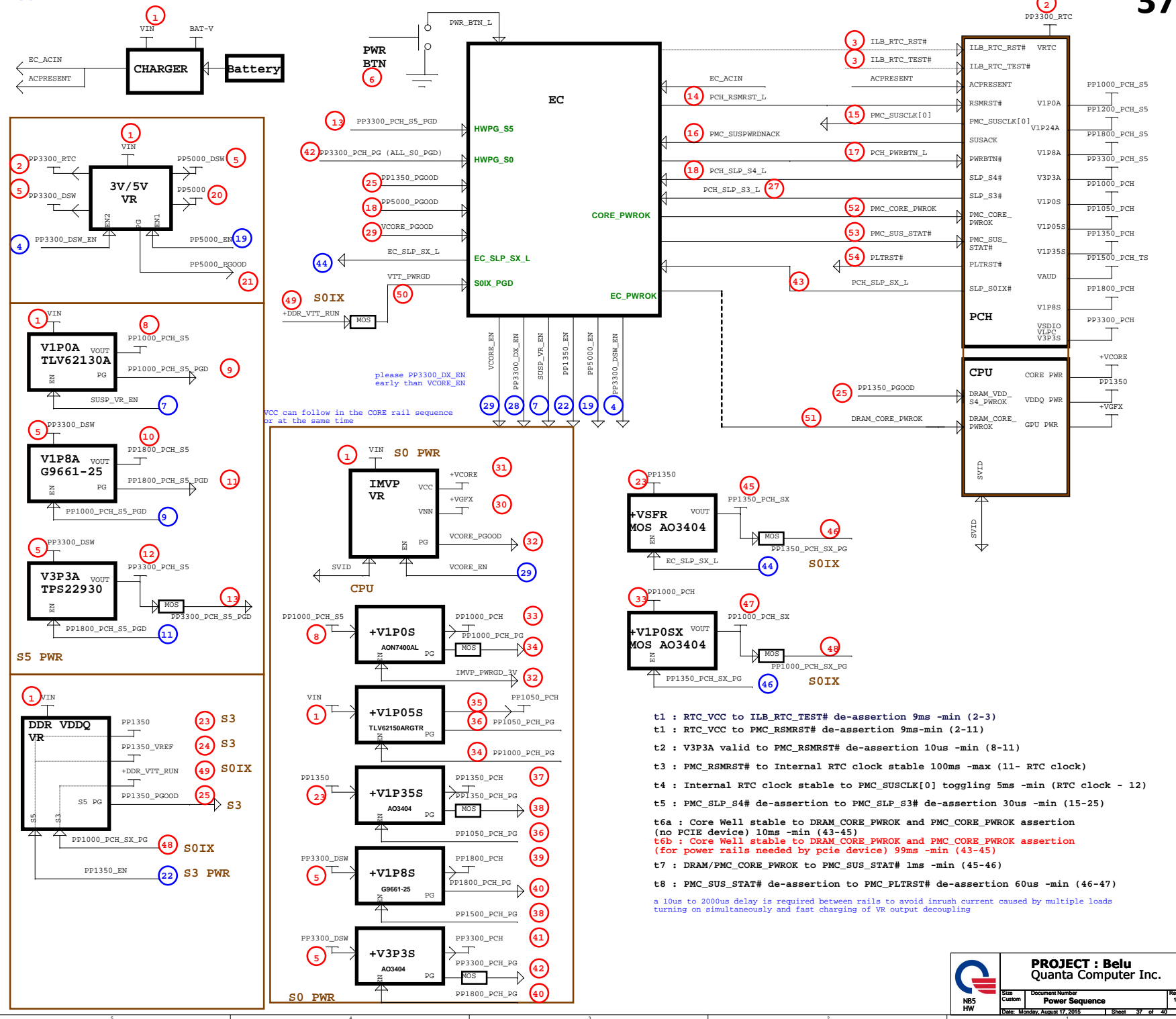




VIN_VCC_CORE VIN_VCC_CORE [33]

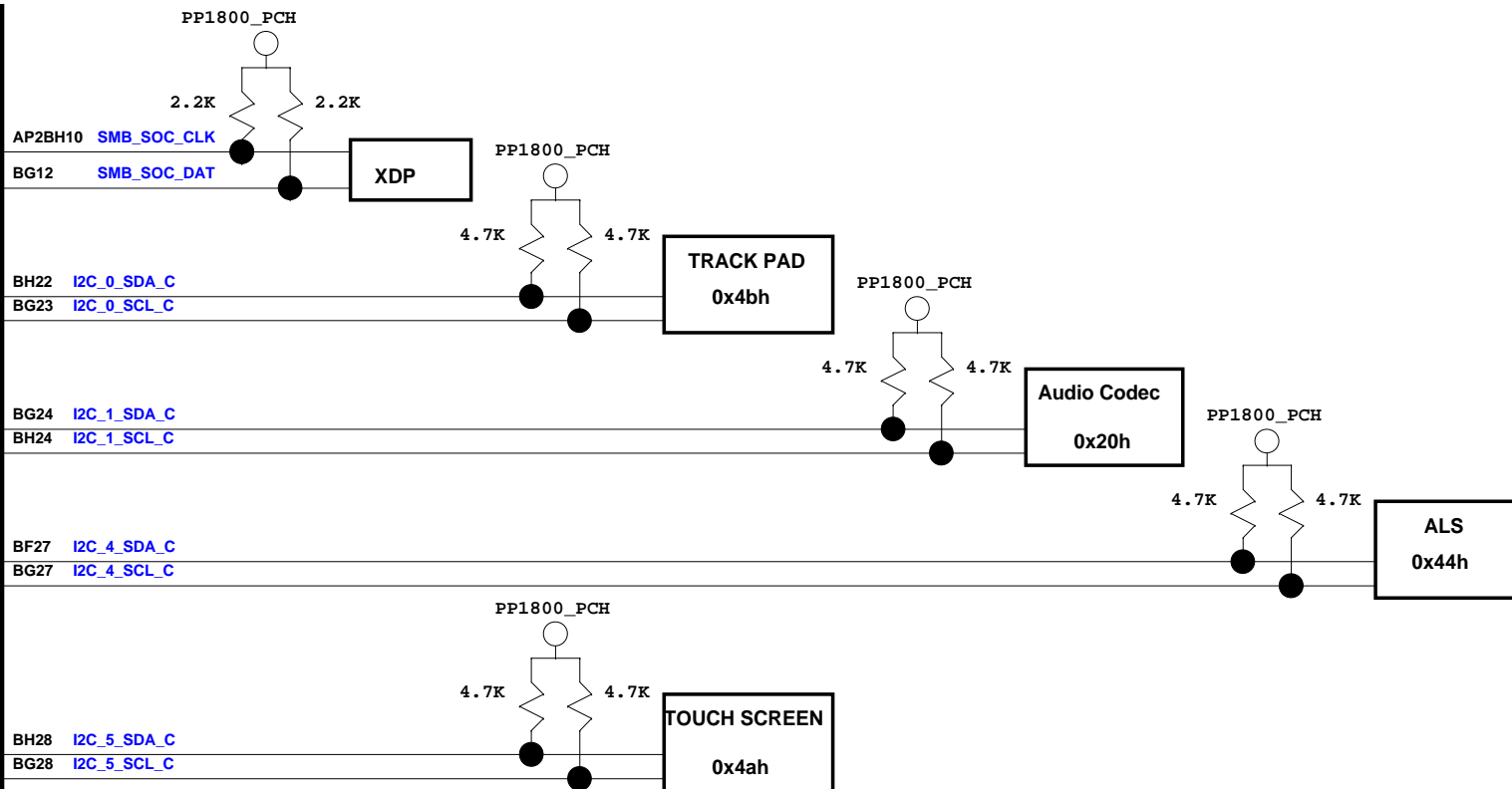
VIN_VCC_GT VIN_VCC_GT [17,25,28,29,31,33,35]



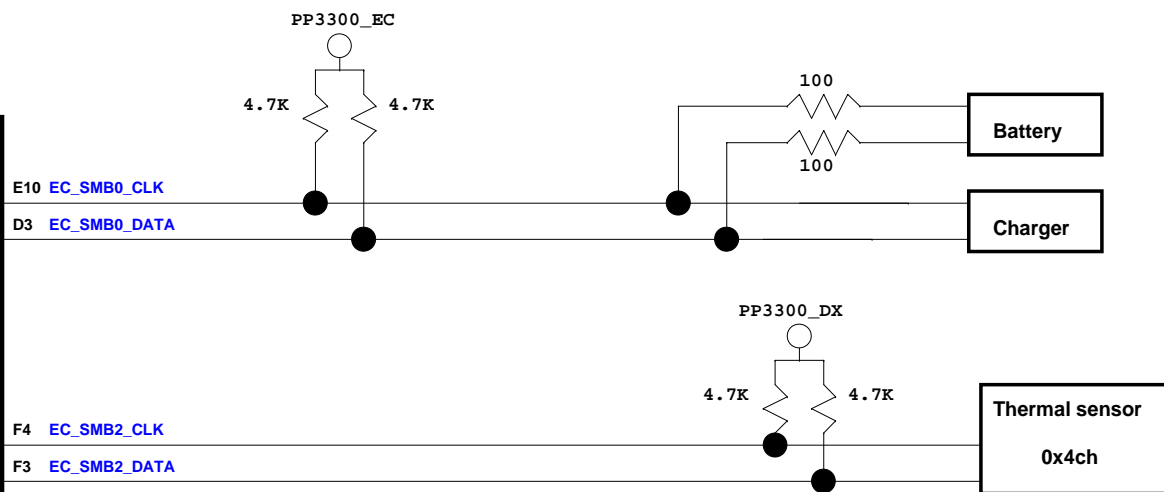


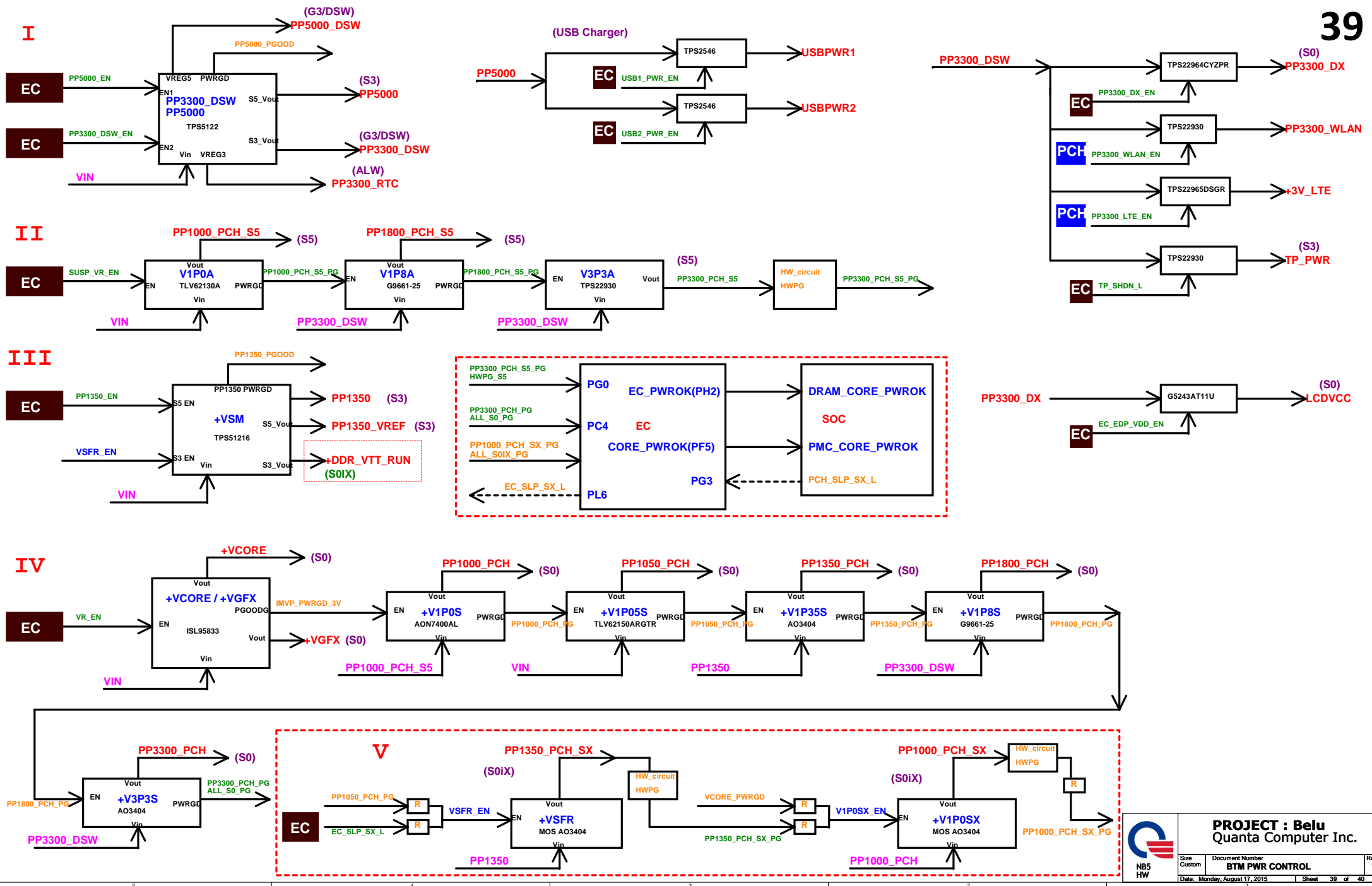
SMBUS
Bay-trail M

I2C



KBC
TI
SMBUS





PROJECT : Belu
Quanta Computer Inc.